



Scalable HPC Communication Capabilities

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HPC The Challenges



Exascale-Class Computer Platforms – Communication Challenges



Challenge	Solution focus
Very large functional unit count ~10M	Scalable communication capabilities: point-to-point & collectives
Large on-"node" functional unit count ~500	Scalable HCA architecture
Deeper memory hierarchies	Cache aware network access
Smaller amounts of memory per functional unit	Low latency, high b/w capabilities
May have functional unit heterogeneity	Support for data heterogeneity
Component failures part of "normal" operation	Resilient and redundant stack
Data movement is expensive	Optimize data movement
Independent remote progress	Independent hardware progress
Power costs	Power aware hardware

Challenges of Scalable HPC Communication Libraries



- Truly asynchronous communication capabilities
 - Two-sided point-to-point
 - One-sided point-to-point
 - Collective Communication
- Truly one-sided remote progress
- System noise mitigation
- Topology awareness

Standardize your Interconnect

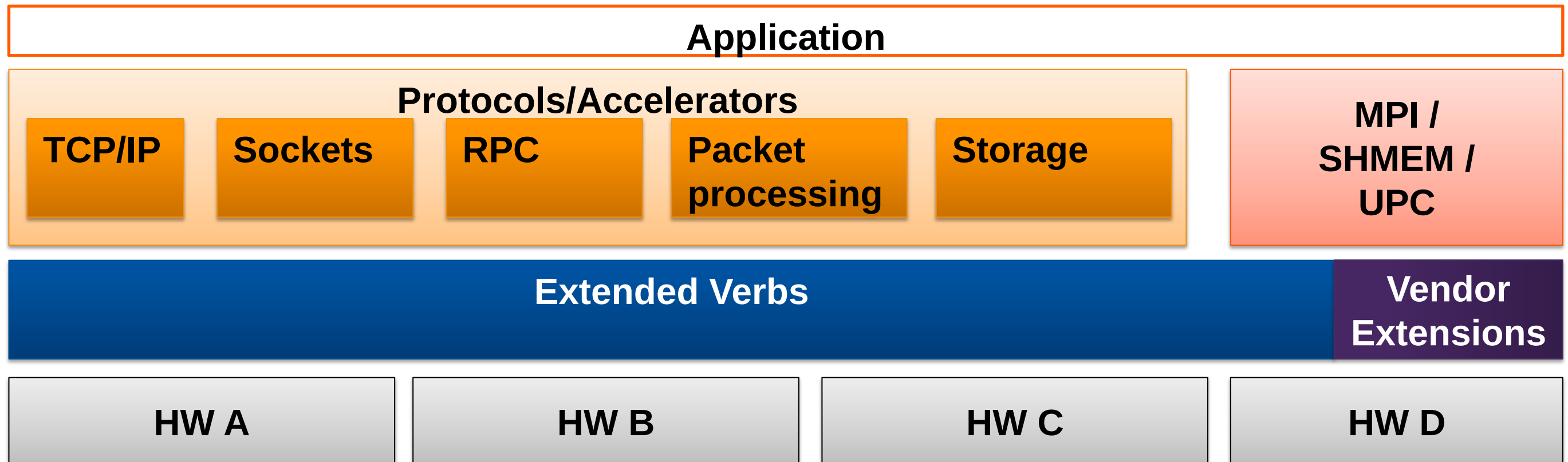


INFINIBAND[®]
TRADE ASSOCIATION



- Standardized wire protocol
 - Mix and match of vertical and horizontal components
 - Ecosystem – build together
- Open-source, extensible interfaces
 - Extend and optimize per applications needs





Speed, Speed, Speed



Technology Roadmap – Always One-Generation Ahead



Terascale

3rd



TOP500 2003
Virginia Tech (Apple)

1st



"Roadrunner"
Mellanox Connected

Petascale



Exascale



2000

2005

2010

2015

2020

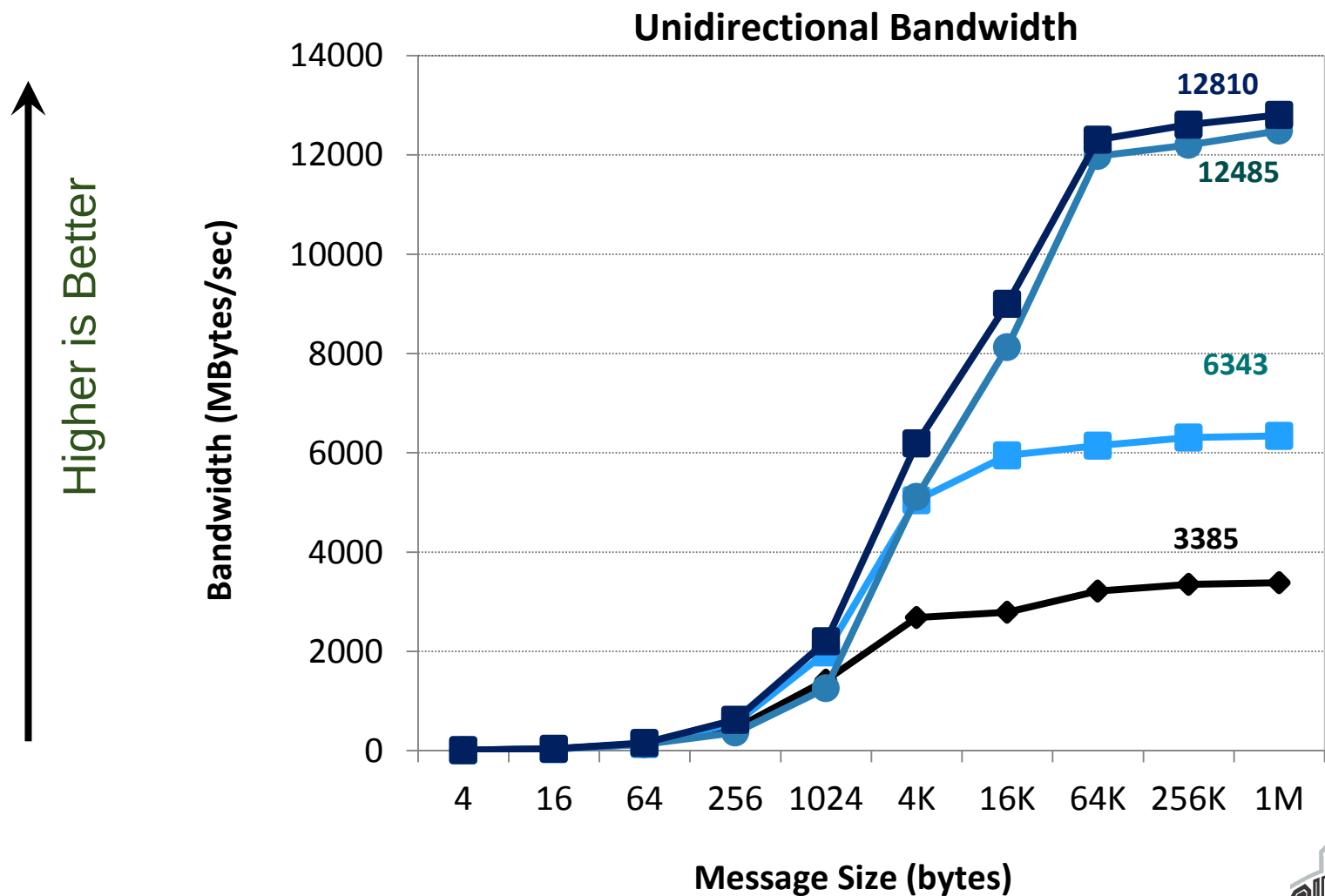
Mellanox Connect-IB The World's Fastest Adapter



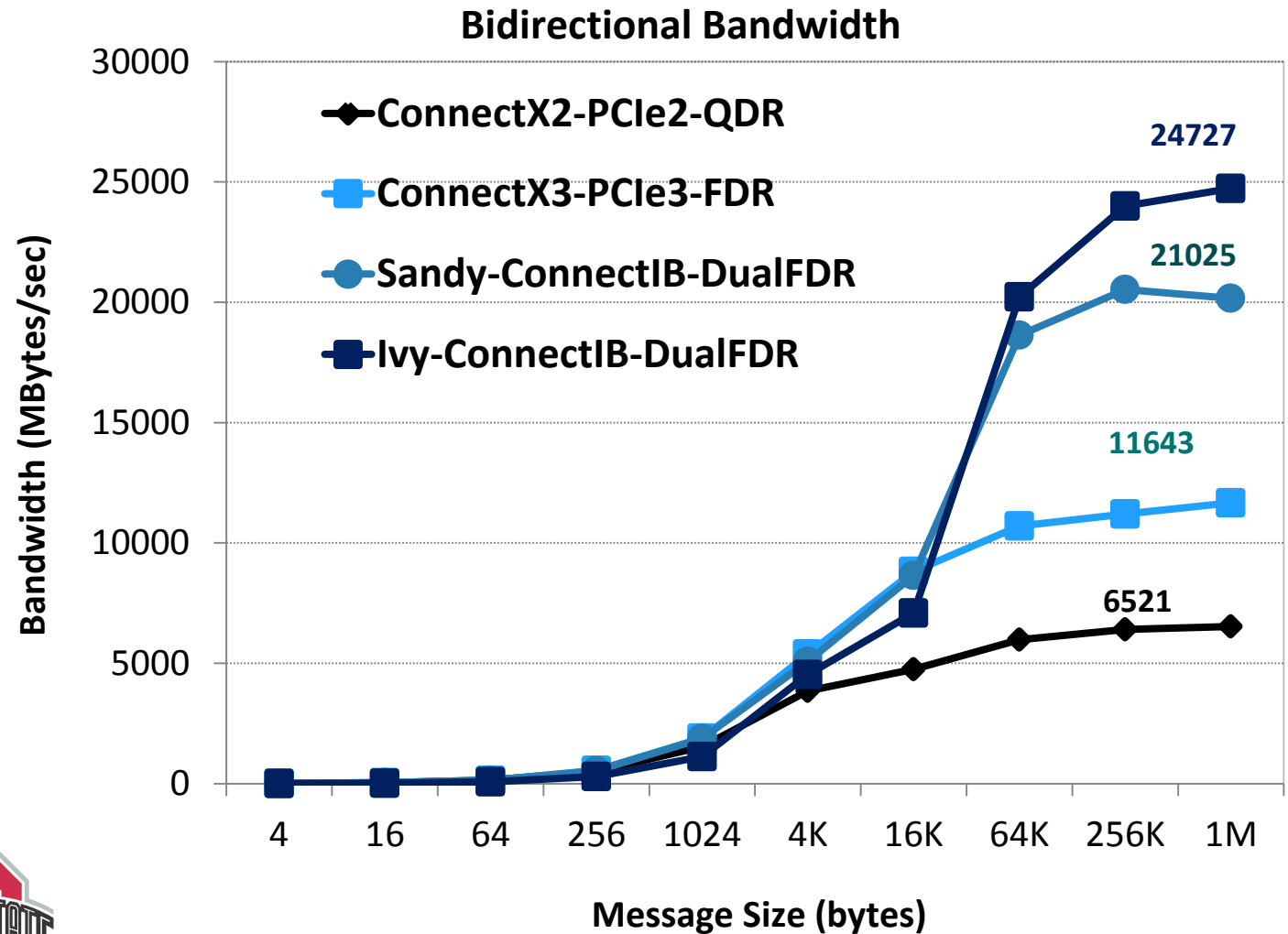
- The 7th generation of Mellanox interconnect adapters
- World's first 100Gb/s interconnect adapter (dual-port FDR 56Gb/s InfiniBand)
- Delivers 137 million messages per second – 4X higher than competition
- Support the new innovative InfiniBand scalable transport – Dynamically Connected



Connect-IB Provides Highest Interconnect Throughput

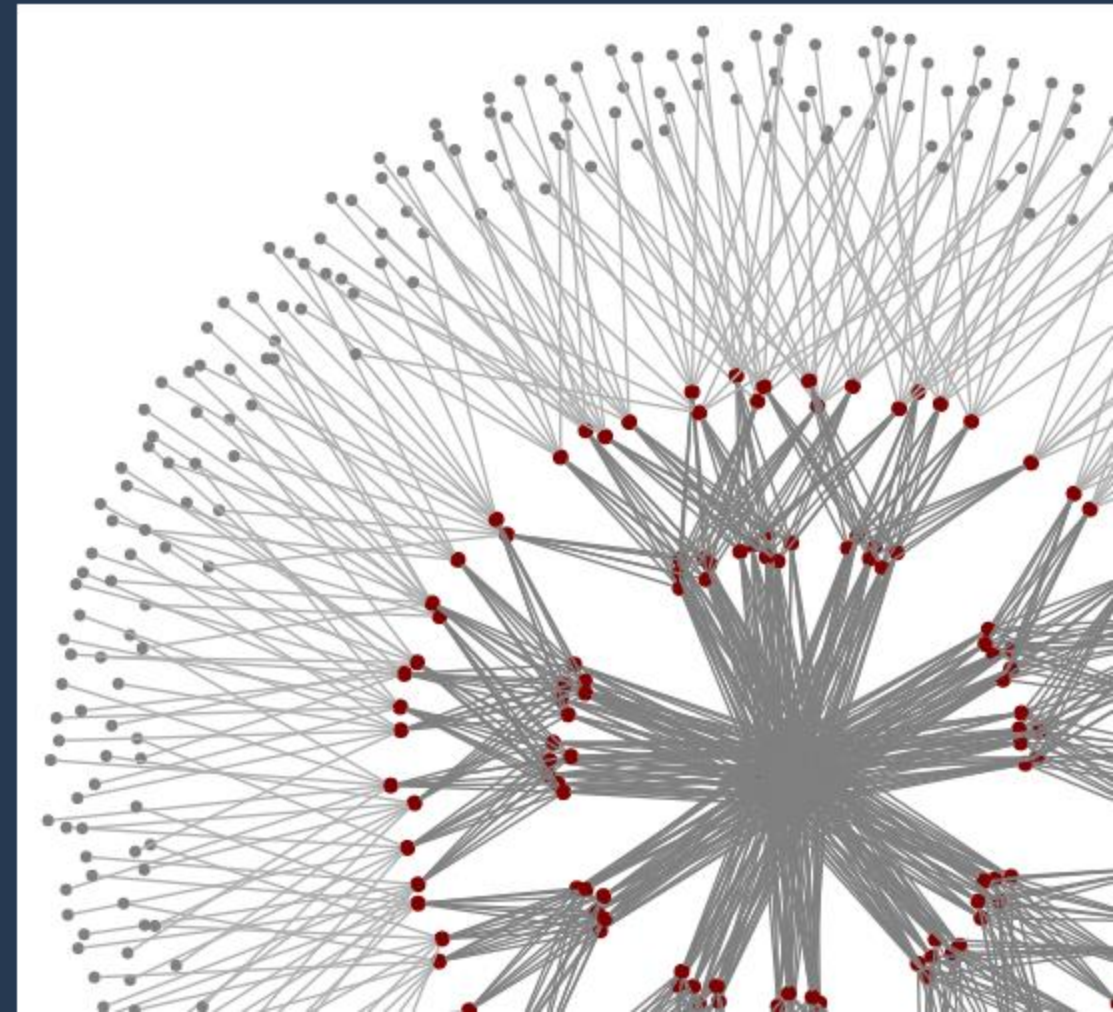


Source: Prof. DK Panda

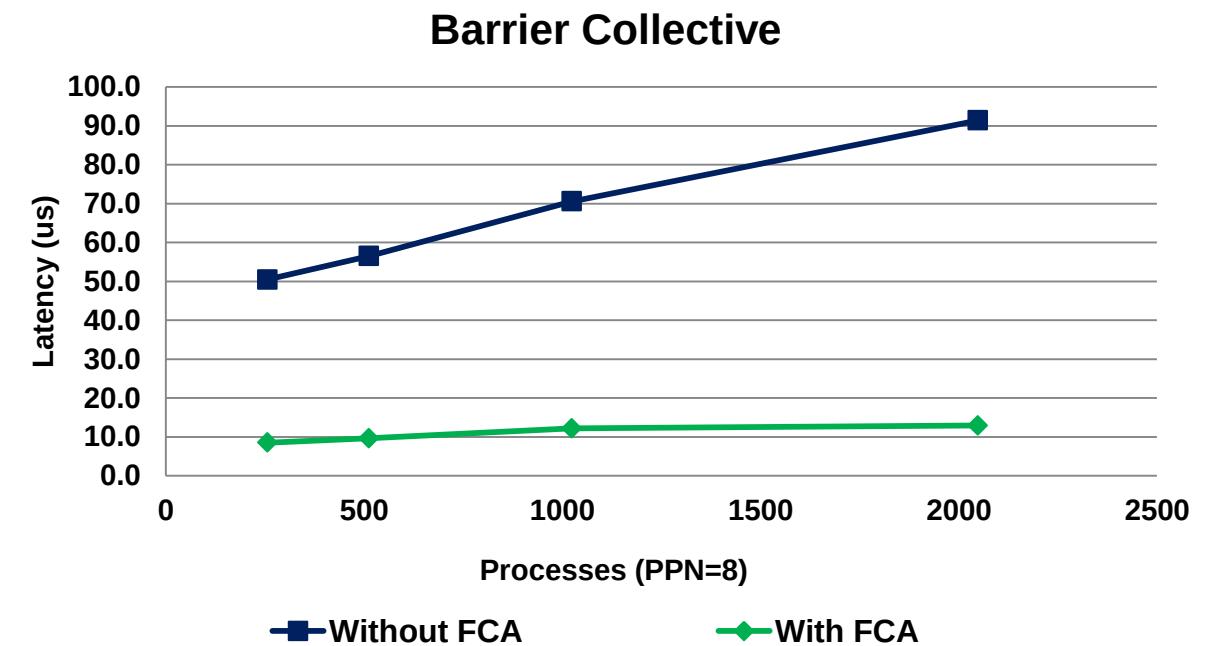
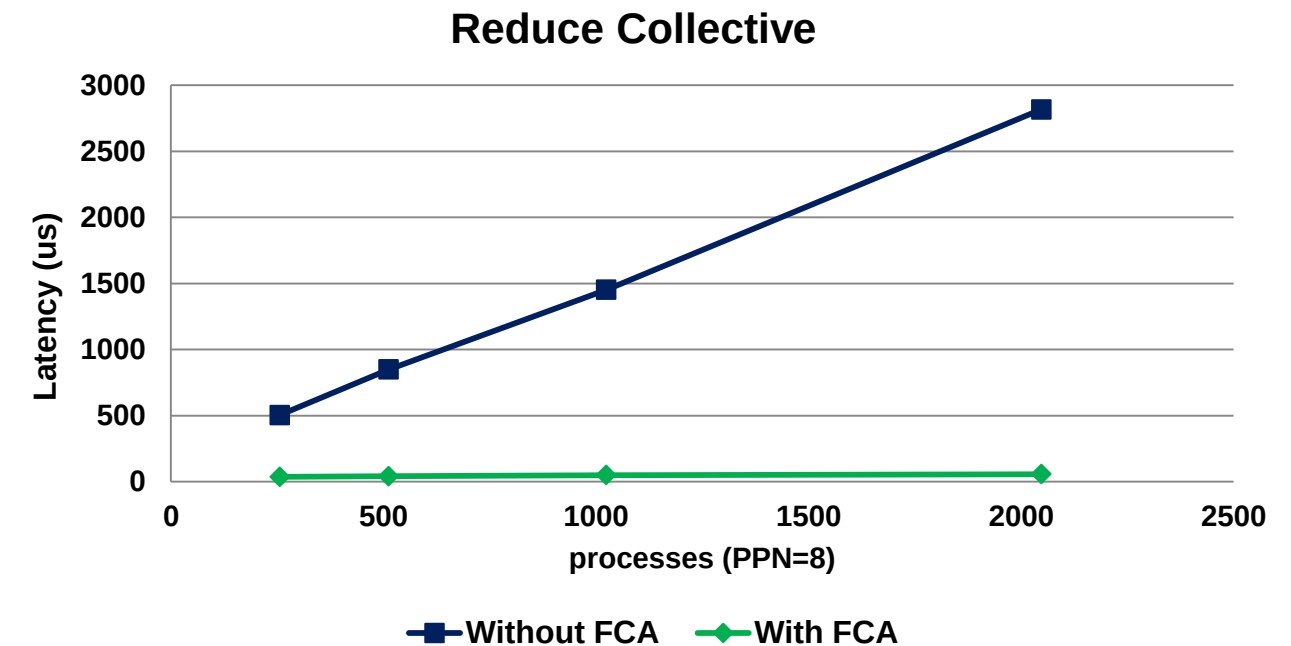


Gain Your Performance Leadership With Connect-IB Adapters

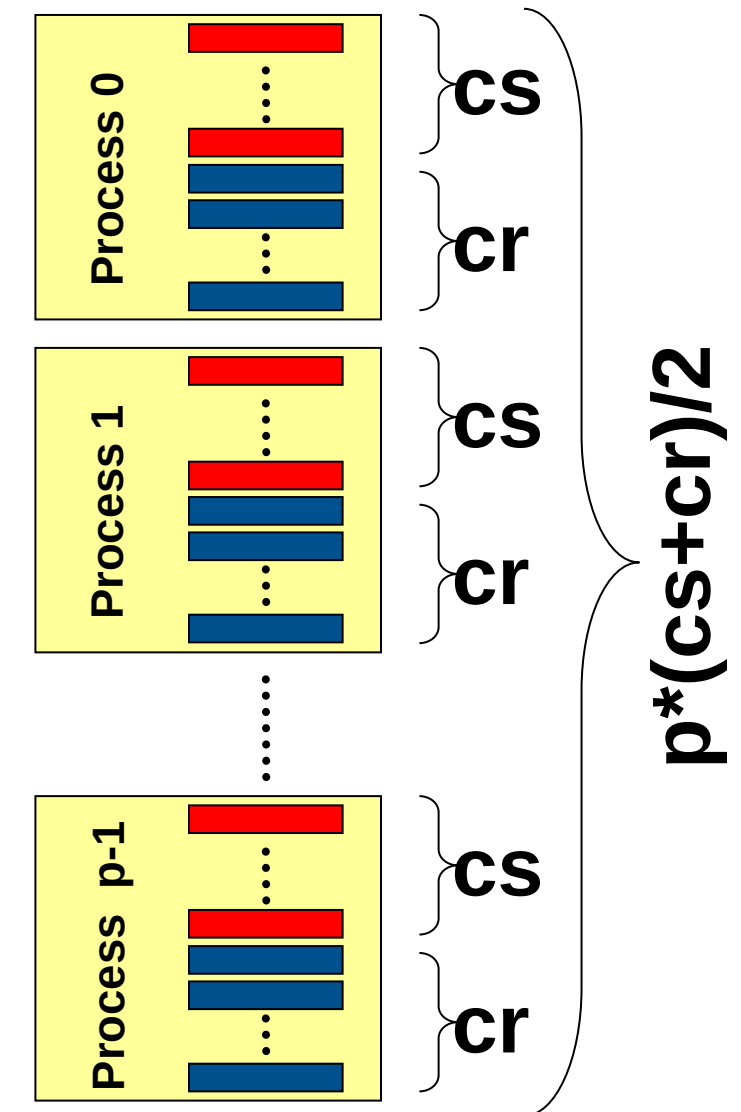
Scalability



- Topology Aware
- Hardware Multicast
- Separate Virtual Fabric
- Offload
- Scalable algorithms



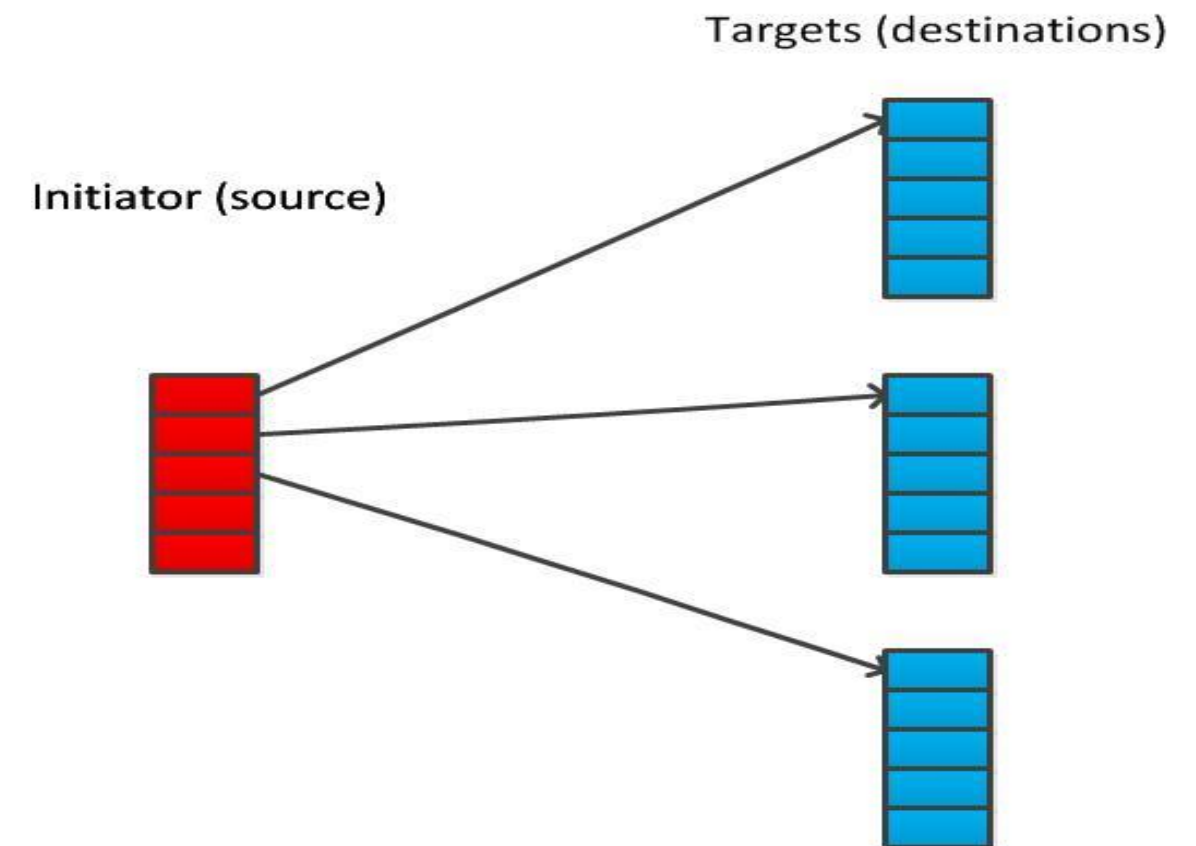
- Dynamic Connectivity
- Each DC Initiator can be used to reach any remote DC Target
- No resources' sharing between processes
 - process controls how many (and can adapt to load)
 - process controls usage model (e.g. SQ allocation policy)
 - no inter-process dependencies
- Resource footprint
 - Function of node and HCA capability
 - Independent of system size
- Fast Communication Setup Time



cs – concurrency of the sender
cr=concurrency of the responder

■ Key objects

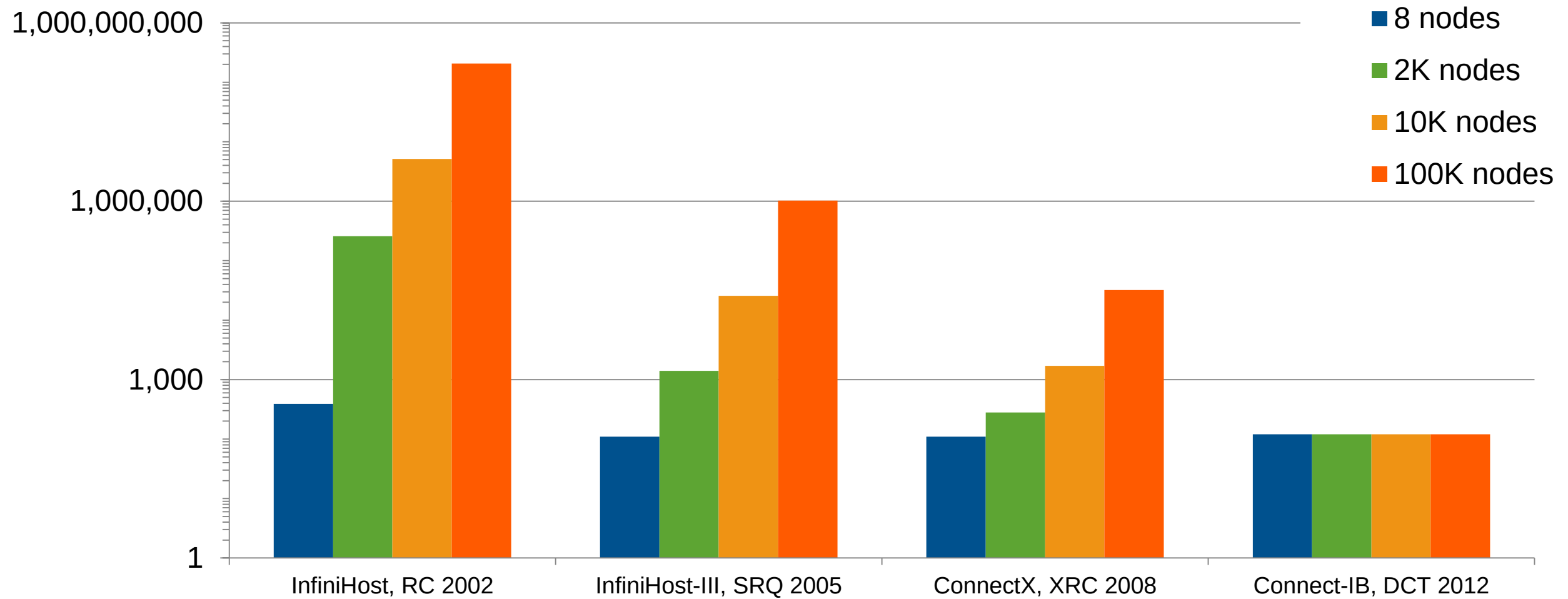
- DC Initiator: Initiates data transfer
- DC Target: Handles incoming data



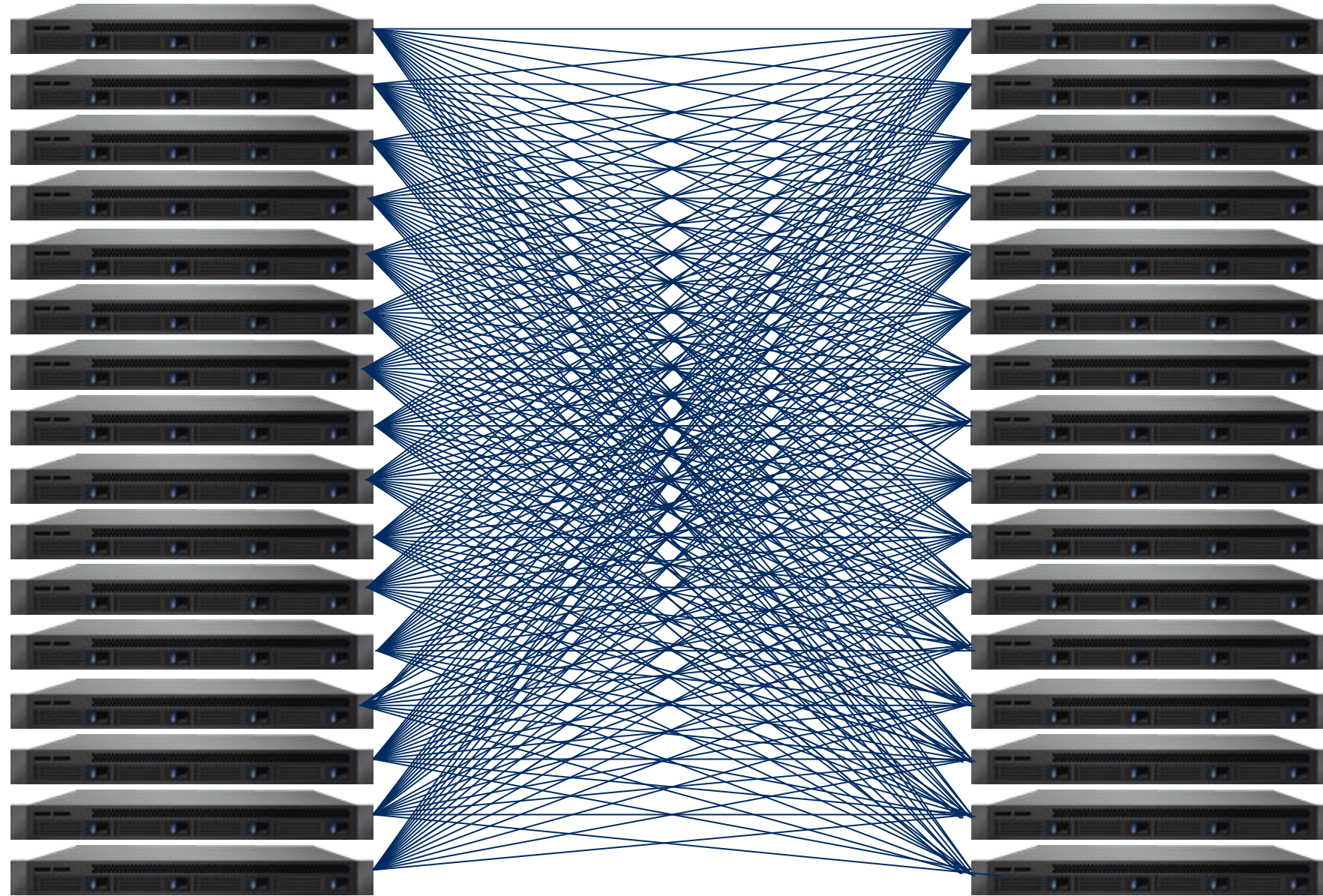
Dynamically Connected Transport – Exascale Scalability



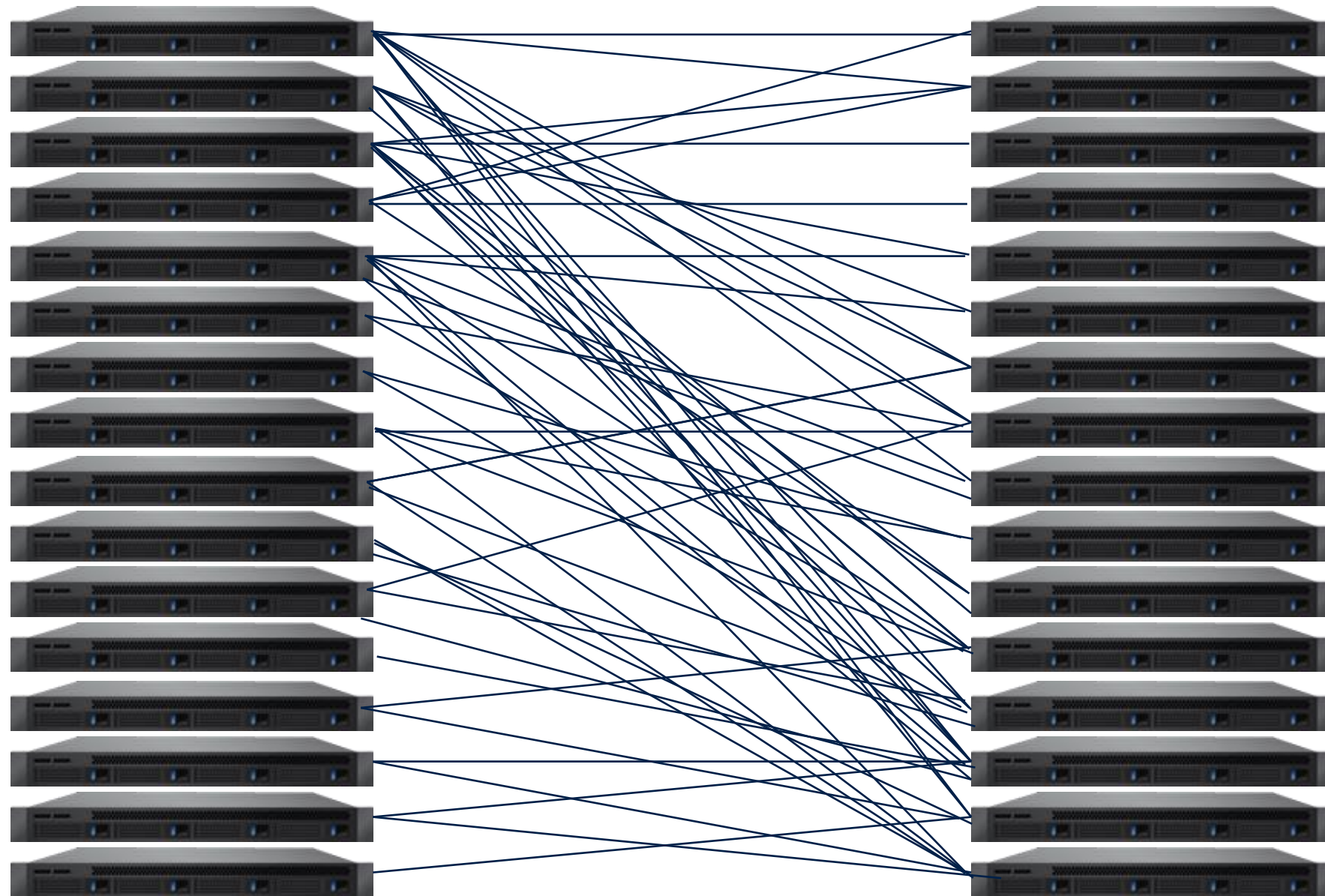
Host Memory Consumption (MB)



Reliable Connection Transport Mode

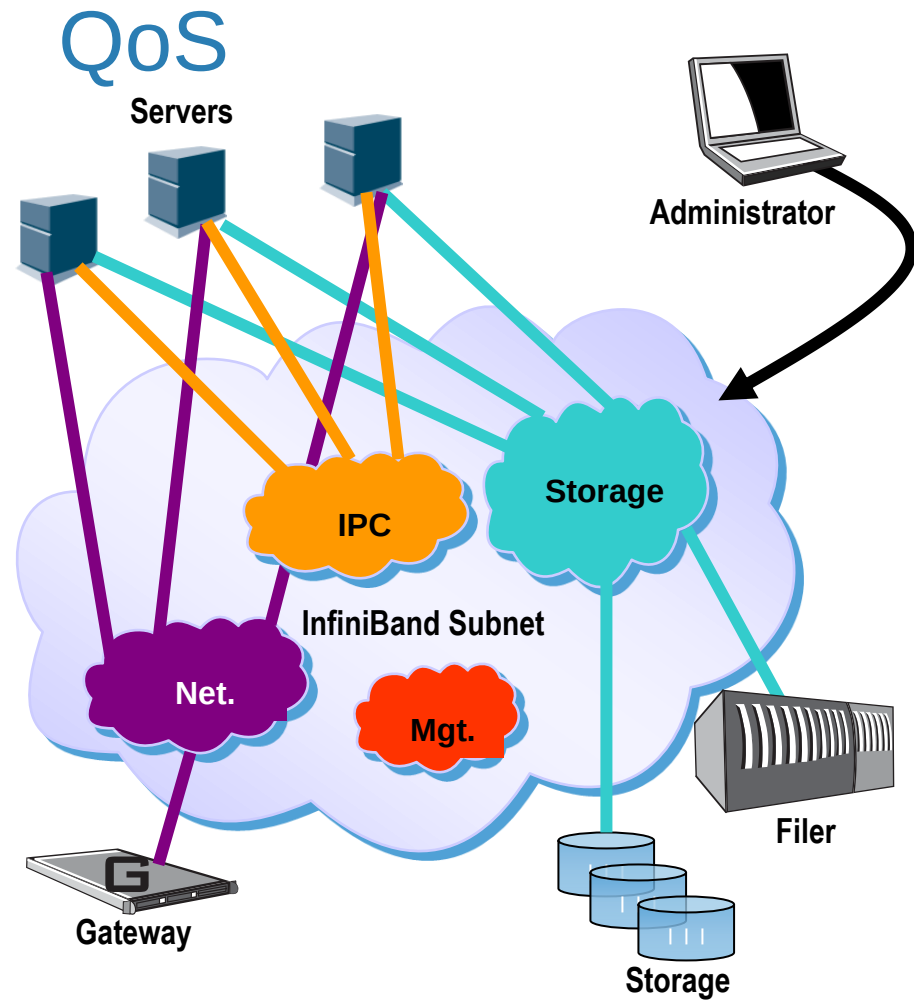


Dynamically Connected Transport Mode

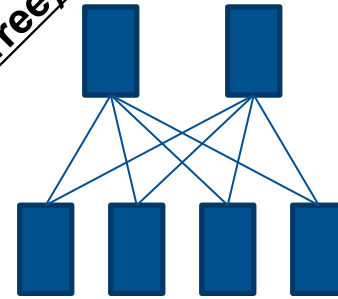


More...

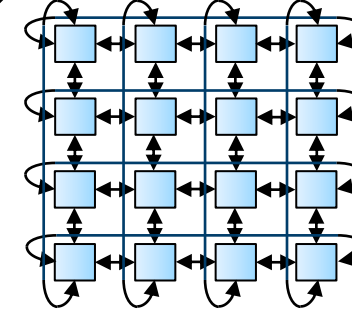
Topologies



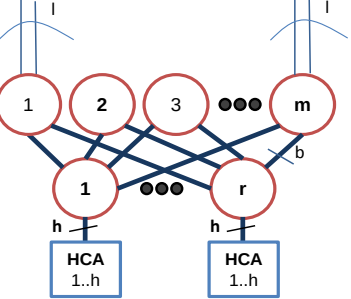
CLOS (Fat Tree)



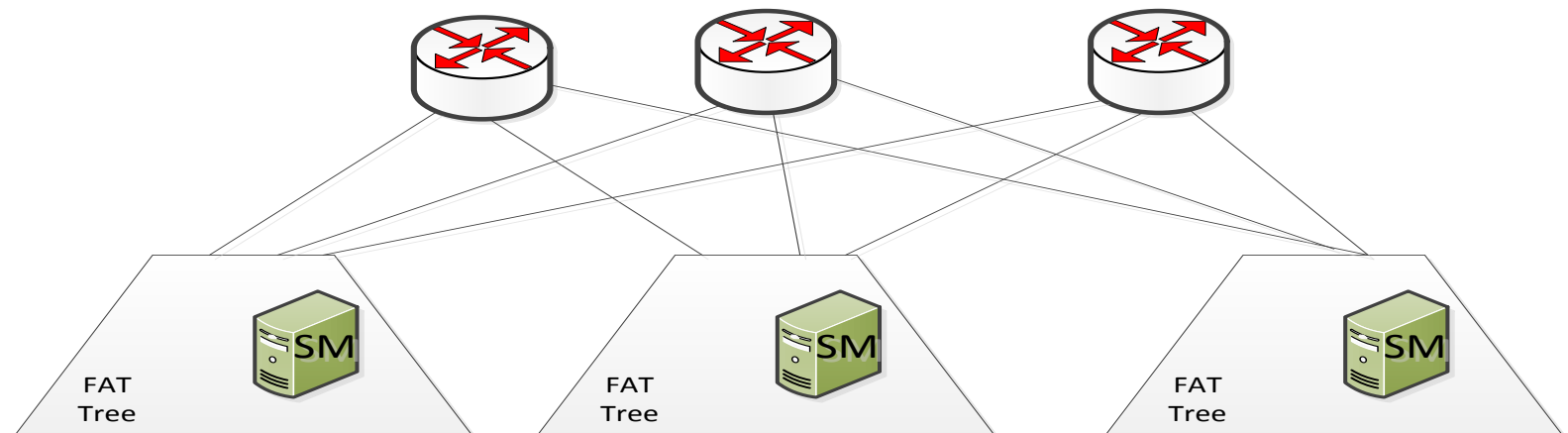
Mesh / 3D Torus



Dragonfly+



Routers



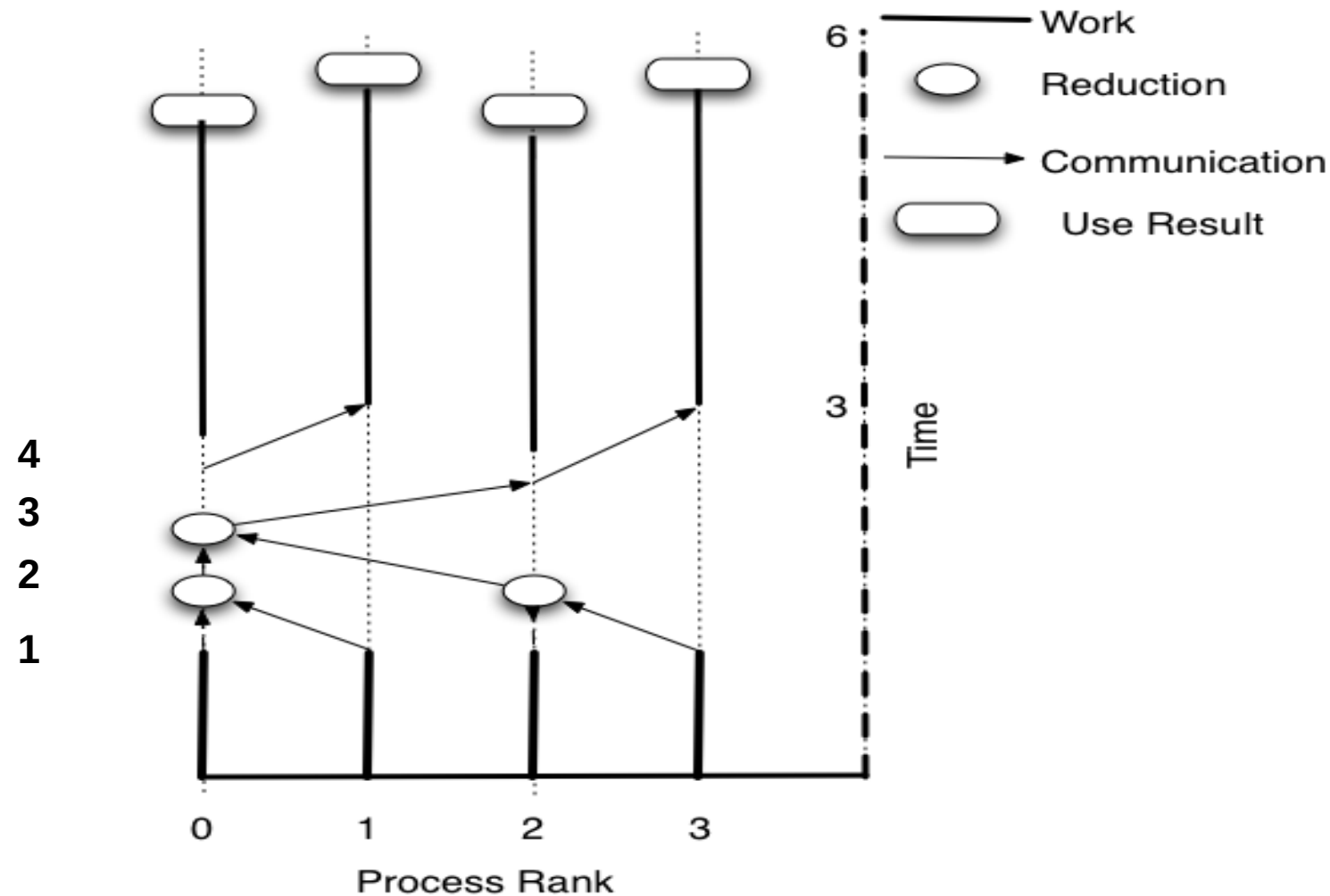
Distance



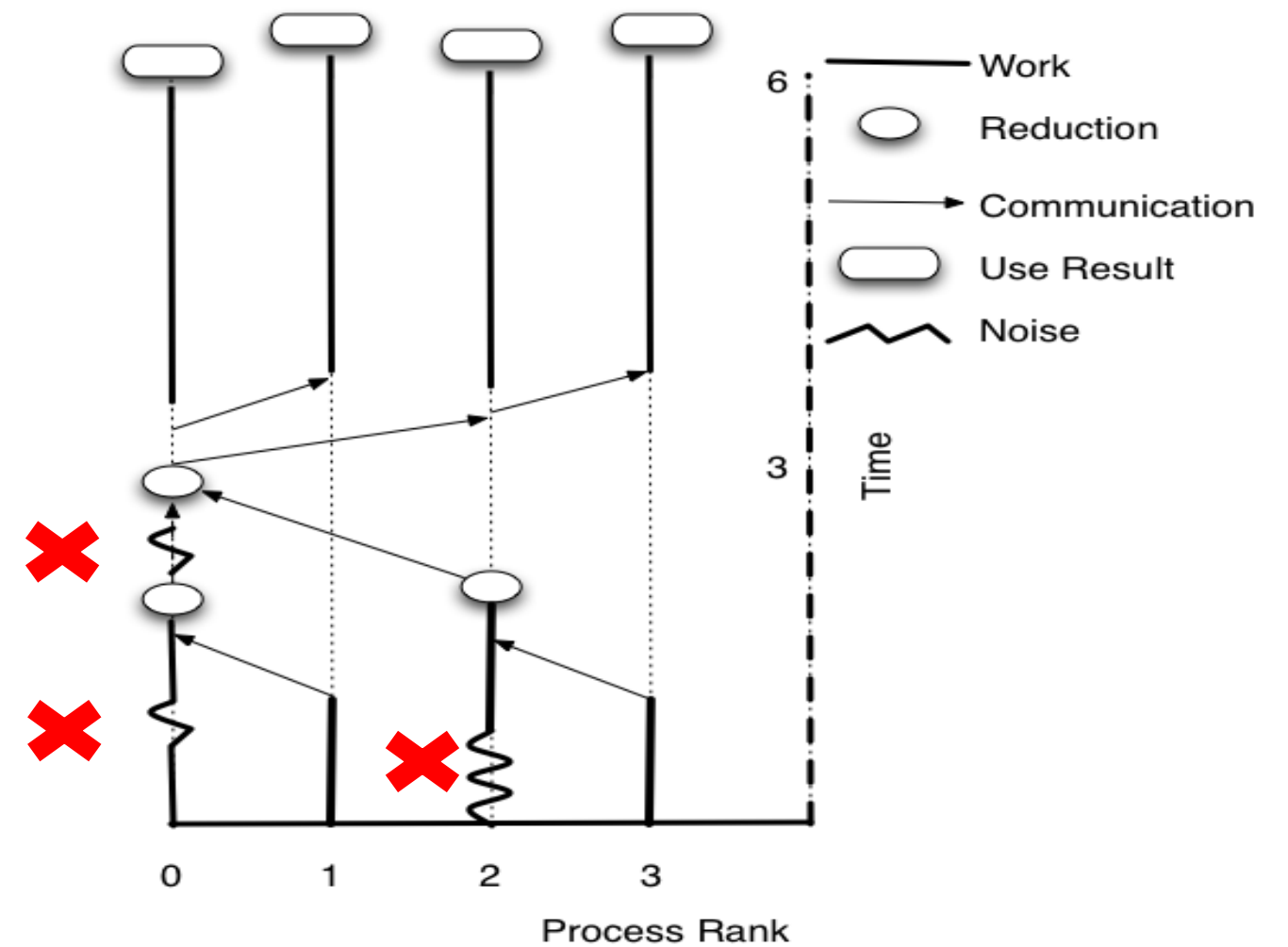
Network Offload

```
0 4 7 1 7 4 3 7 0 4 7 8 4 1 0 0 1 8 1 4 7 5 5 0 8 7 2 9 4 1 0 0 0 4 7 1 7
1 8 2 3 4 1 0 4 1 8 2 4 6 6 2 1 6 4 0 9 9 4 1 3 7 8 7 8 6 6 2 1 1 8 2 3 4
9 9 9 5 9 9 3 9 9 9 9 1 9 8 0 6 8 1 3 8 8 6 6 2 4 5 4 4 9 8 0 6 9 9 9 5 9
4 4 3 4 8 8 5 8 4 4 3 9 9 0 4 5 4 5 2 6 7 5 5 0 5 4 8 5 9 0 4 5 4 4 3 4 8
9 9 1 0 0 7 4 4 9 9 1 8 8 4 1 1 6 9 1 0 5 9 4 0 6 8 0 5 4 8 4 1 1 6 9 9 1 0 0
8 8 4 6 1 9 6 5 8 8 4 4 8 9 9 0 5 8 3 5 1 6 1 4 4 2 8 7 6 8 9 9 0 5 8 8 4 6 1
6 0 8 2 3 0 0 2 3 5 3 0 9 4 2 0 6 0 8 2 3 0 0 2 0 2 1 1 2 3 0 0 9 1 8 6 3
1 5 5 3 2 6 1 0 6 4 5 3 8 9 0 1 1 5 5 3 2 6 1 0 1 1 5 1 4 2 0 6 7 2 9 5 6
5 4 9 0 1 5 4 1 5 9 1 6 7 8 1 9 5 4 9 0 1 5 4 1 6 6 6 6 5 1 6 5 0 5 2 7 4 5
4 4 4 1 8 1 9 4 4 8 3 5 4 7 4 8 4 4 4 1 8 1 9 4 5 5 5 5 1 6 1 1 9 7 9 6 4
4 9 9 4 7 6 6 4 9 0 2 4 9 8 4 7 9 4 9 9 4 7 6 6 4 1 1 1 3 4 5 4 6 8 8 5 4 9
9 8 8 9 4 4 5 9 6 6 1 9 8 4 9 4 8 9 8 8 9 4 4 5 9 4 4 2 2 6 6 6 5 5 5 9 6 6
8 4 4 8 9 5 1 8 4 8 5 6 8 0 0 8 9 7 8 4 4 8 9 5 1 8 4 6 5 0 1 5 5 5 1 0 9 6 5 8
7 6 5 7 8 1 6 4 9 4 4 5 4 4 2 4 8 4 7 6 5 7 8 1 6 4 9 5 1 5 5 1 1 1 3 1 7 2 4 4
4 5 4 8 4 3 5 1 8 6 9 7 6 8 1 1 0 4 5 4 8 4 3 5 1 8 1 0 1 6 3 3 4 2 6 8 1 6 6
6 1 5 9 6 0 1 6 4 5 5 4 5 7 6 6 4 6 1 5 9 6 0 1 6 4 6 2 6 5 5 2 2 7 5 2 6 8 5
2 6 3 0 5 5 4 5 4 1 9 3 9 5 5 6 2 6 3 0 5 5 4 5 4 8 0 5 1 4 5 5 5 0 1 4 4 4
1 8 4 1 0 6 6 1 9 3 8 1 9 0 1 4 1 8 4 1 0 6 6 1 5 1 4 5 2 1 1 9 5 6 2 6 9
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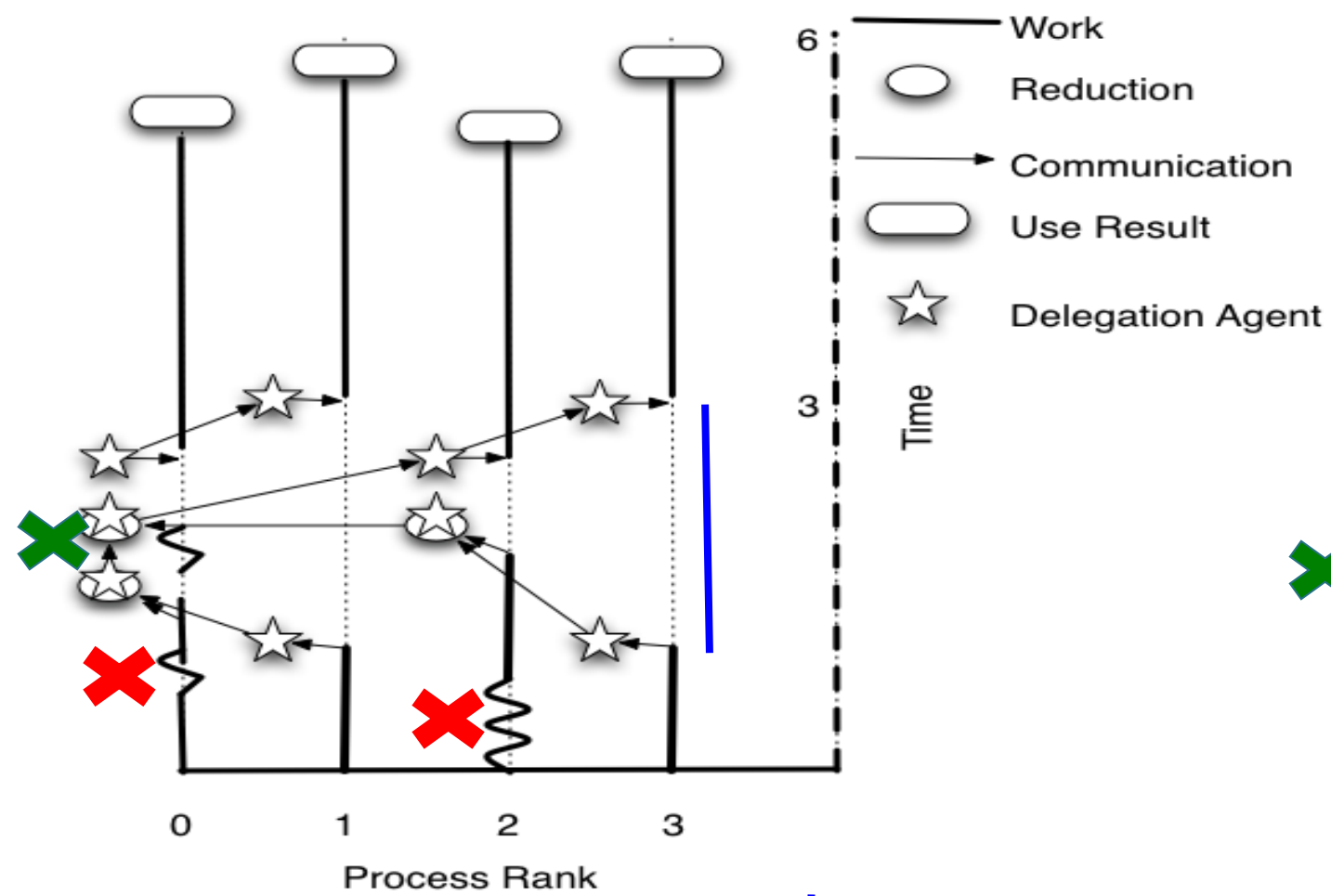
Ideal Algorithm



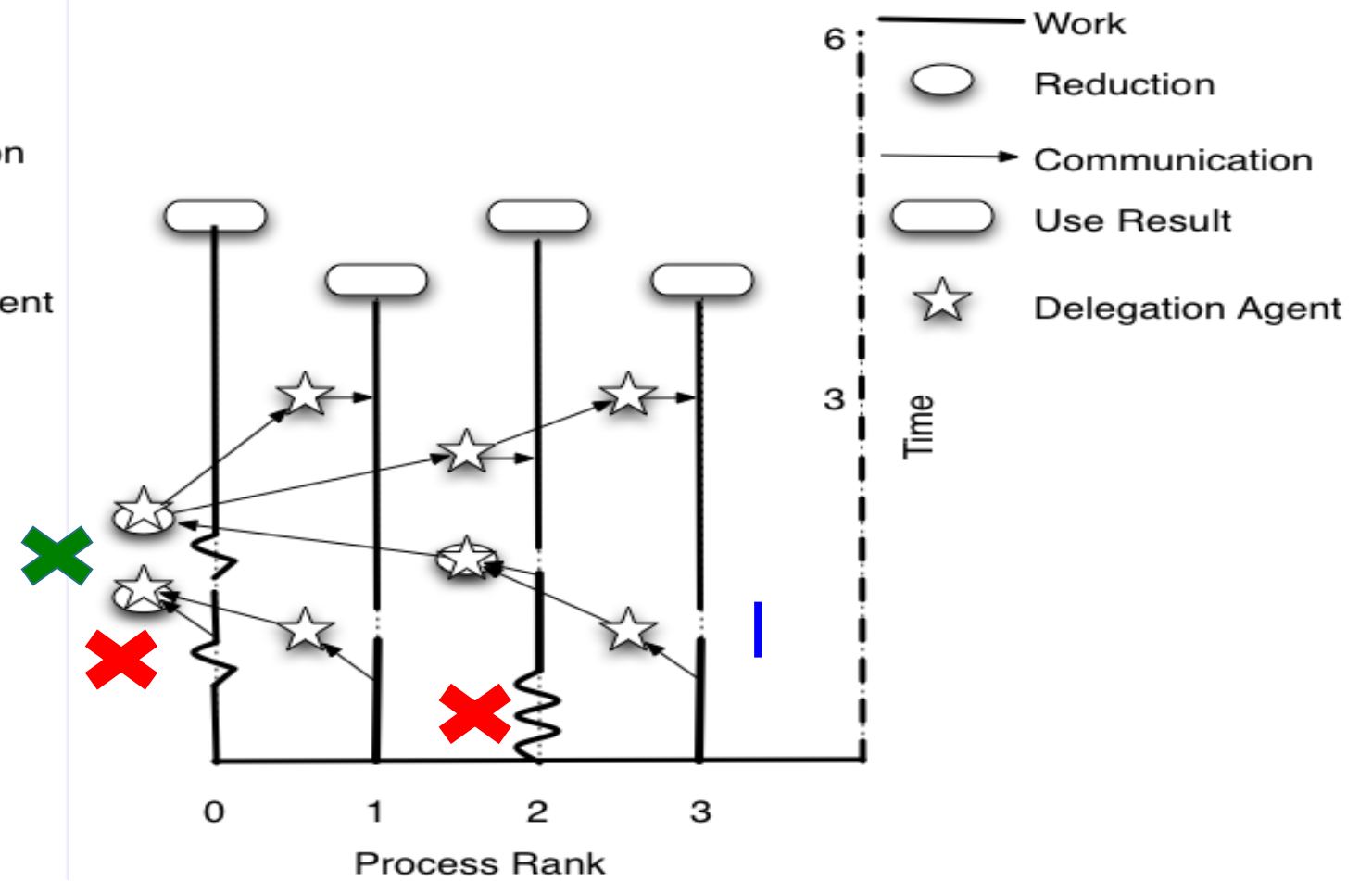
Impact of System Noise



Offloaded Algorithm



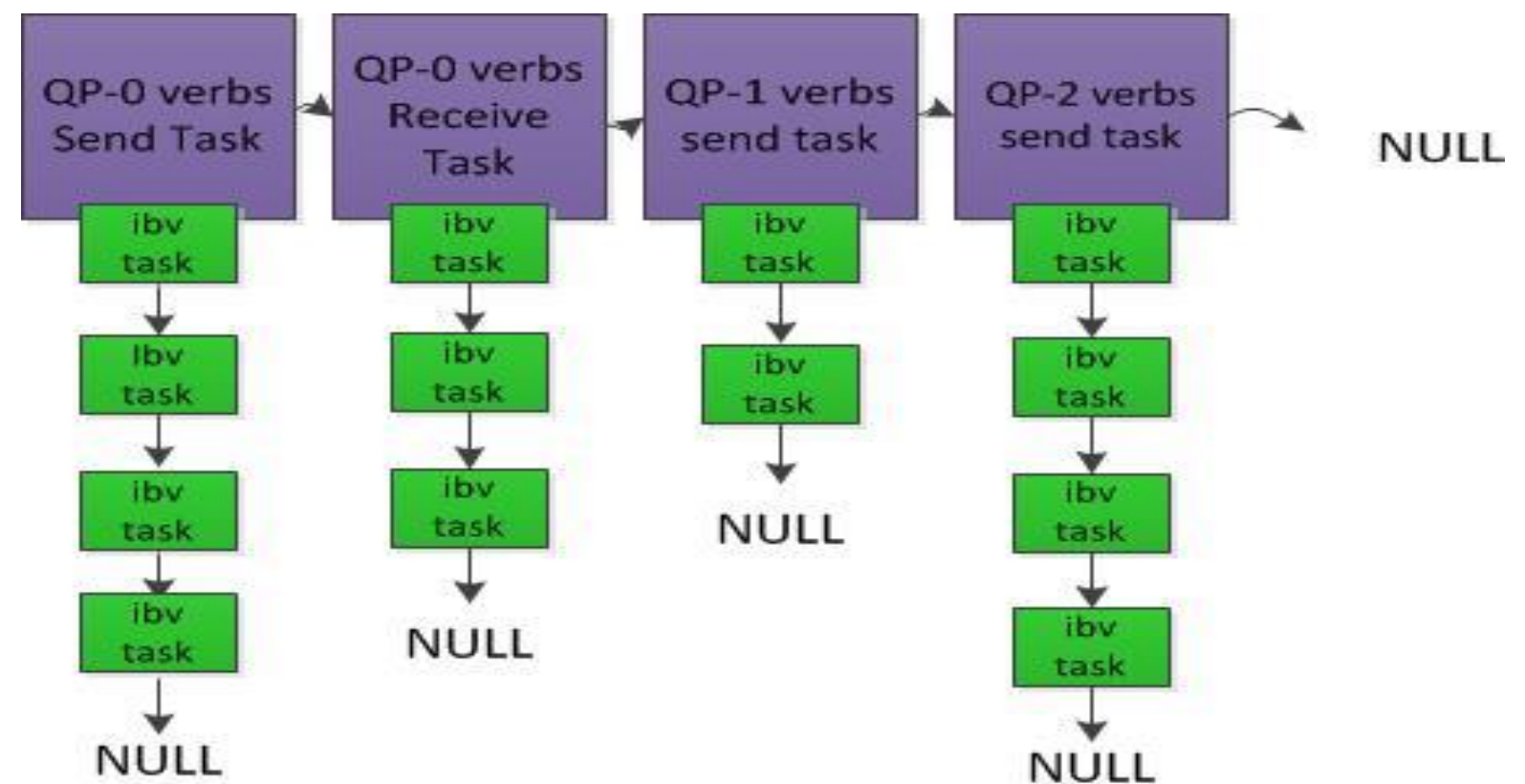
Nonblocking Algorithm



- Communication processing

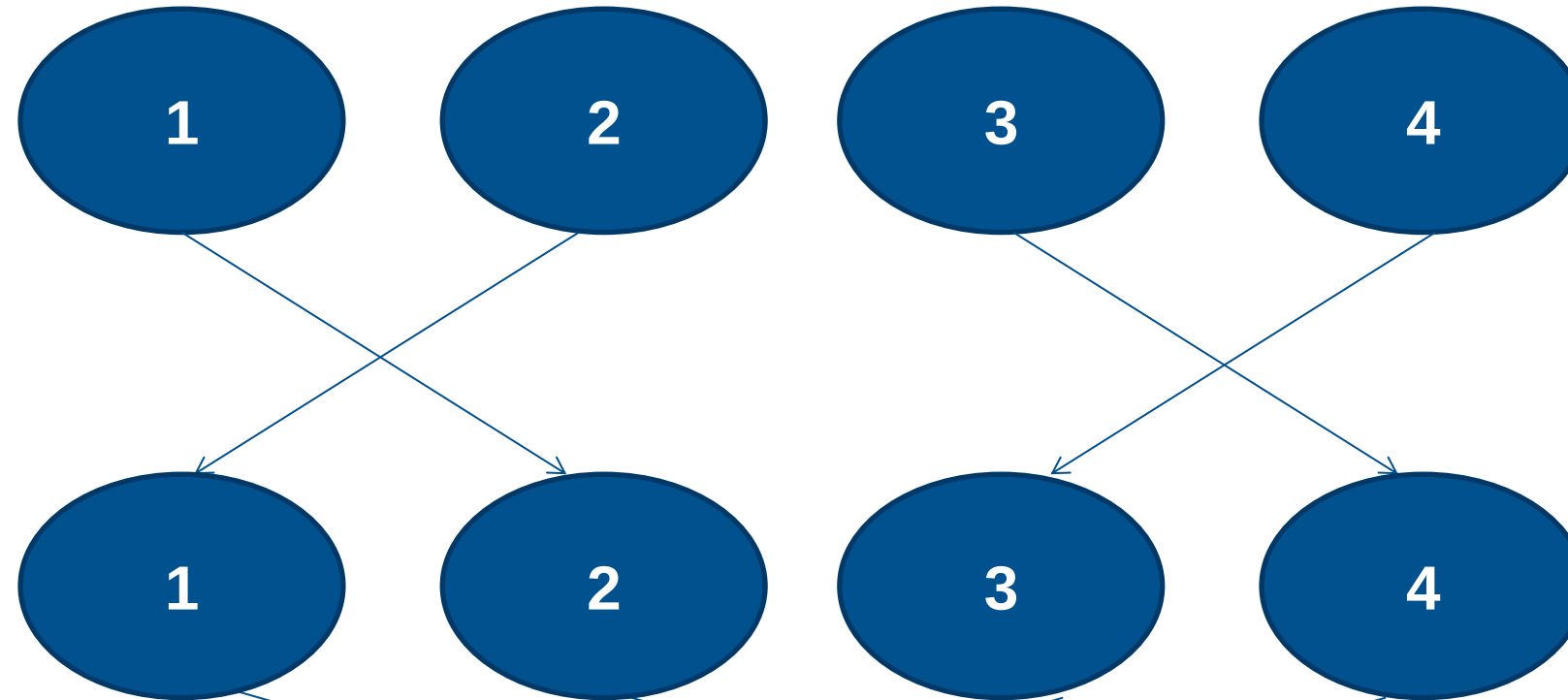
- Scalable collective communication
- Asynchronous communication
- Manage communication by communication resources
- Avoid system noise

- Task list
- Target QP for task
- Operation
 - Send
 - Wait for completions
 - Enable
 - Calculate

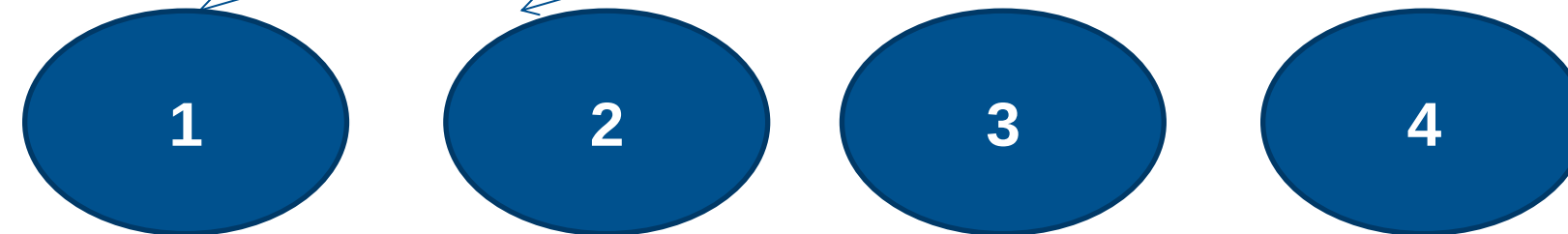


Example – Four Process Recursive Doubling

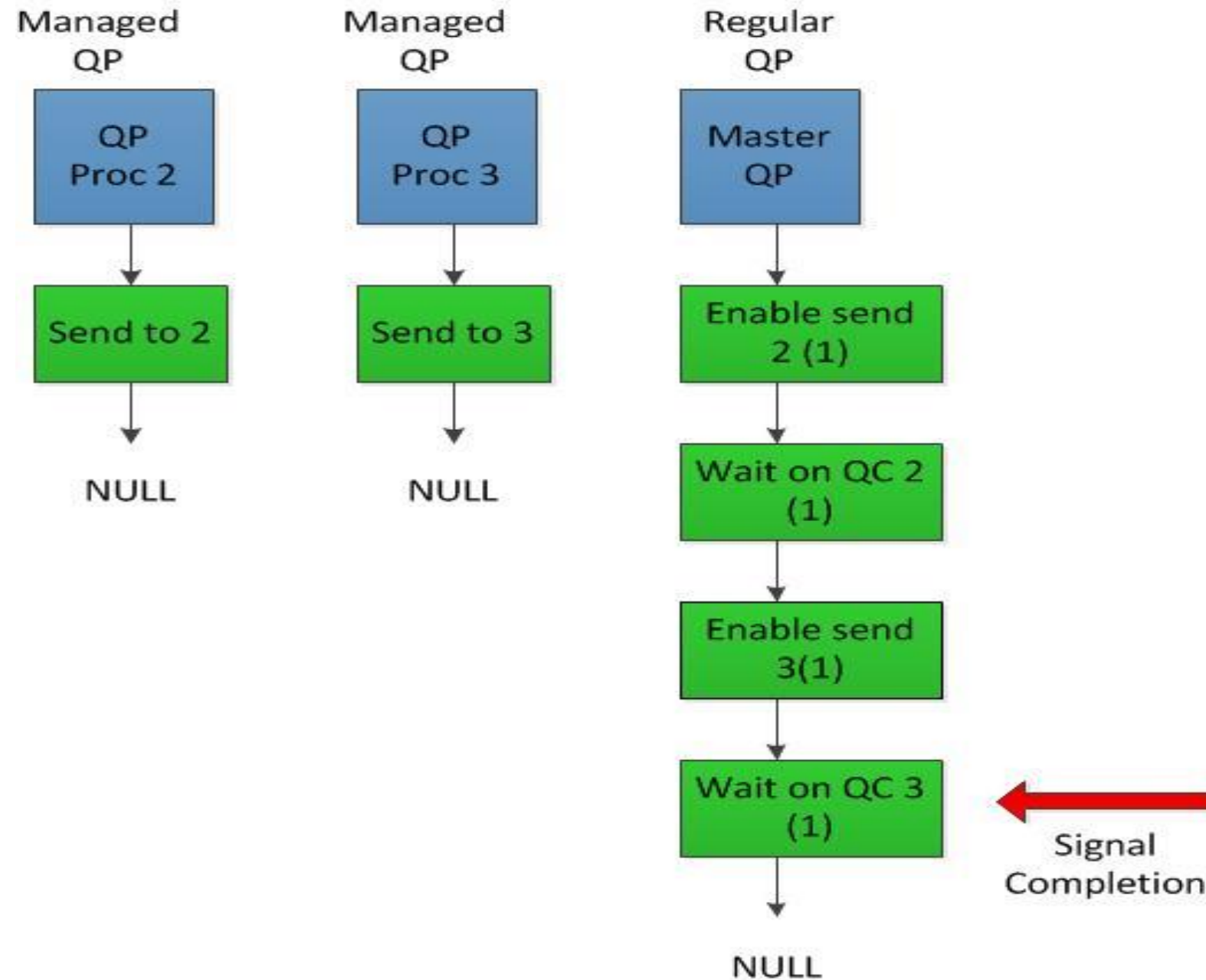
Step 1



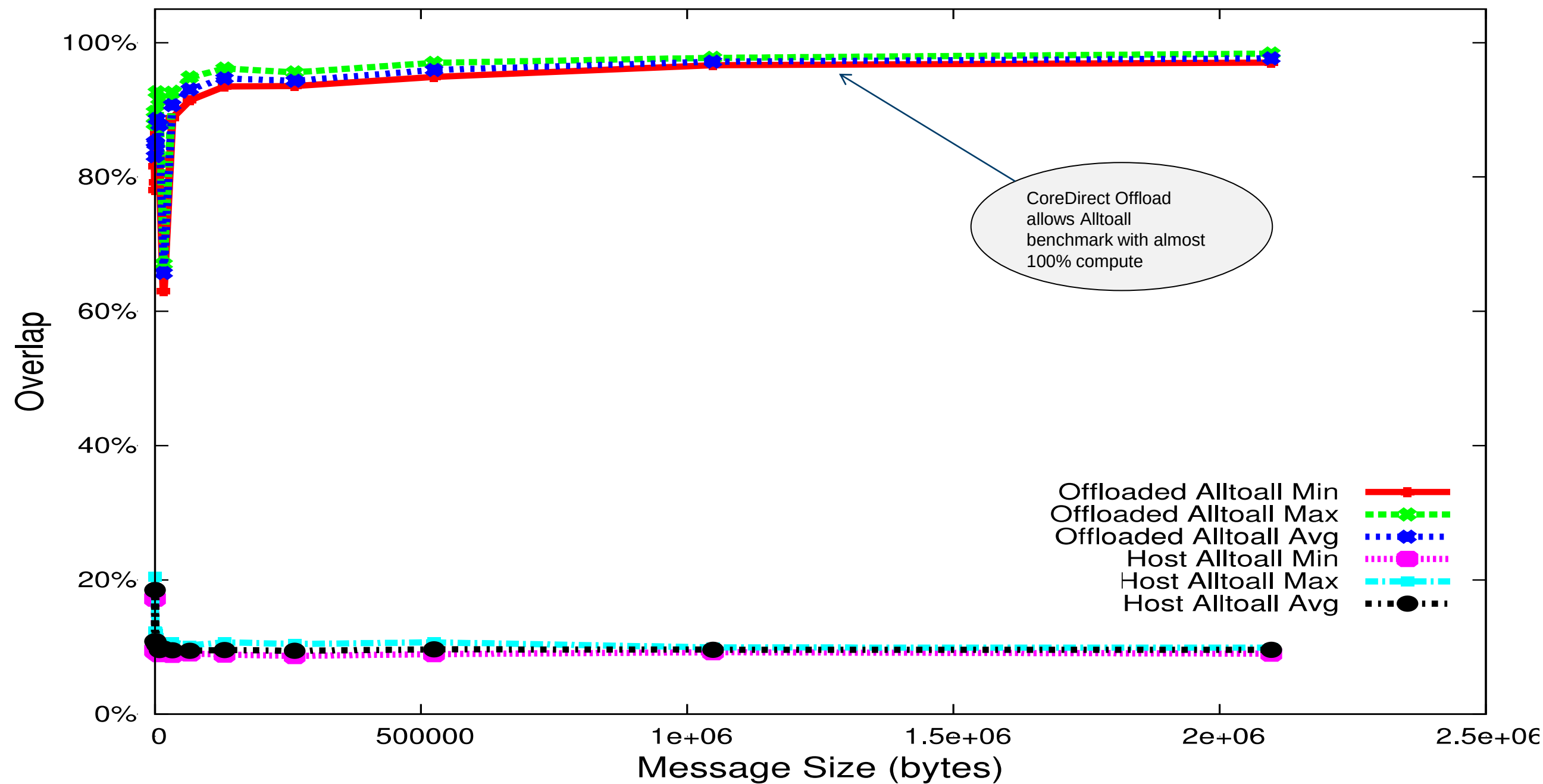
Step 2



Four Process Barrier Example – Using Managed Queues – Rank 0

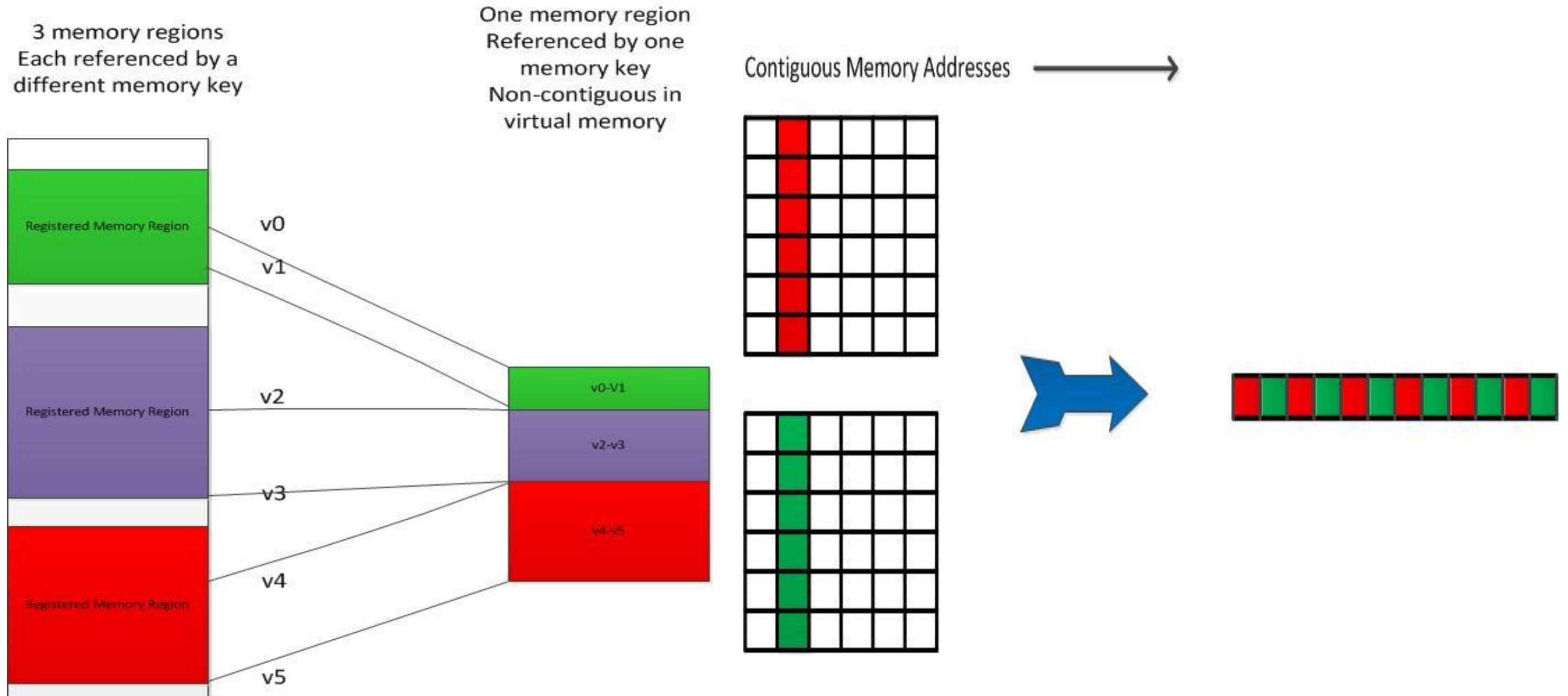


Nonblocking Alltoall (Overlap-Wait) Benchmark

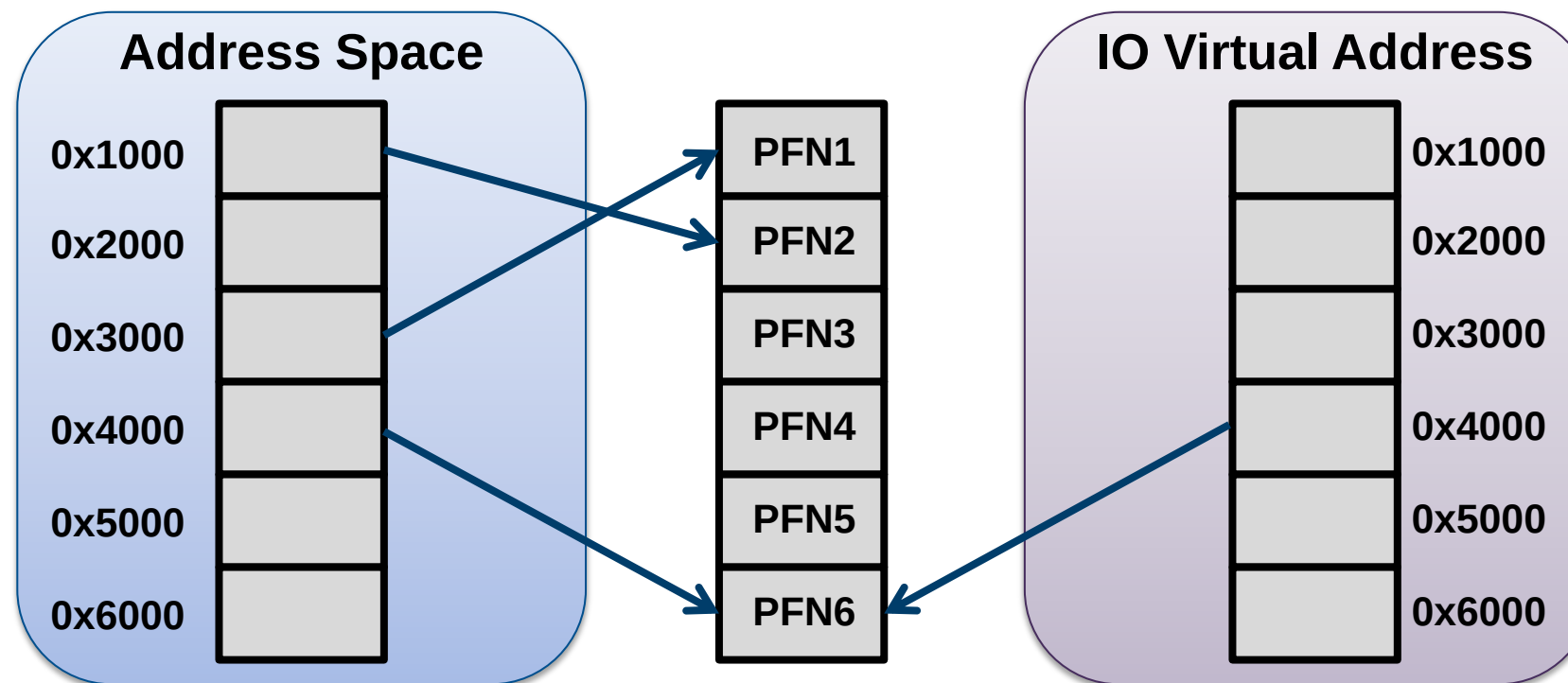


- Support combining contiguous registered memory regions into a single memory region. H/W treats them as a single contiguous region (and handles the non-contiguous regions)
- For a given memory region, supports non-contiguous access to memory, using a regular structure representation – base pointer, element length, stride, repeat count.
 - Can combine these from multiple different memory keys
- Memory descriptors are created by posting WQE's to fill in the memory key
- Supports local and remote non-contiguous memory access
 - Eliminates the need for some memory copies

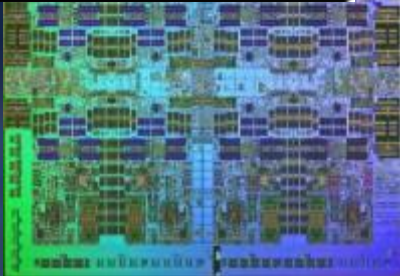
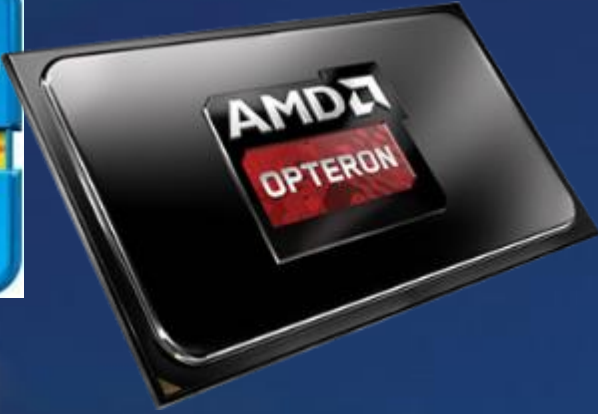
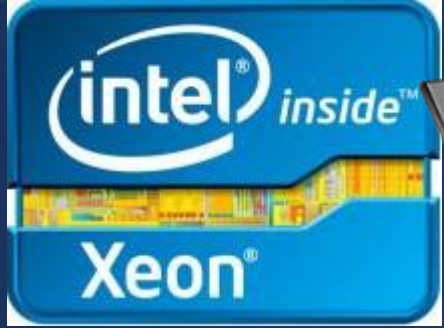
Optimizing Non Contiguous Memory Transfers



- No memory pinning, no memory registration, no registration caches!
- Advantages
 - Greatly simplified programming
 - Unlimited MR sizes
 - Physical memory optimized to hold current working set



Connecting Compute Elements



Receive

Transmit

GPUDirect 1.0

InfiniBand

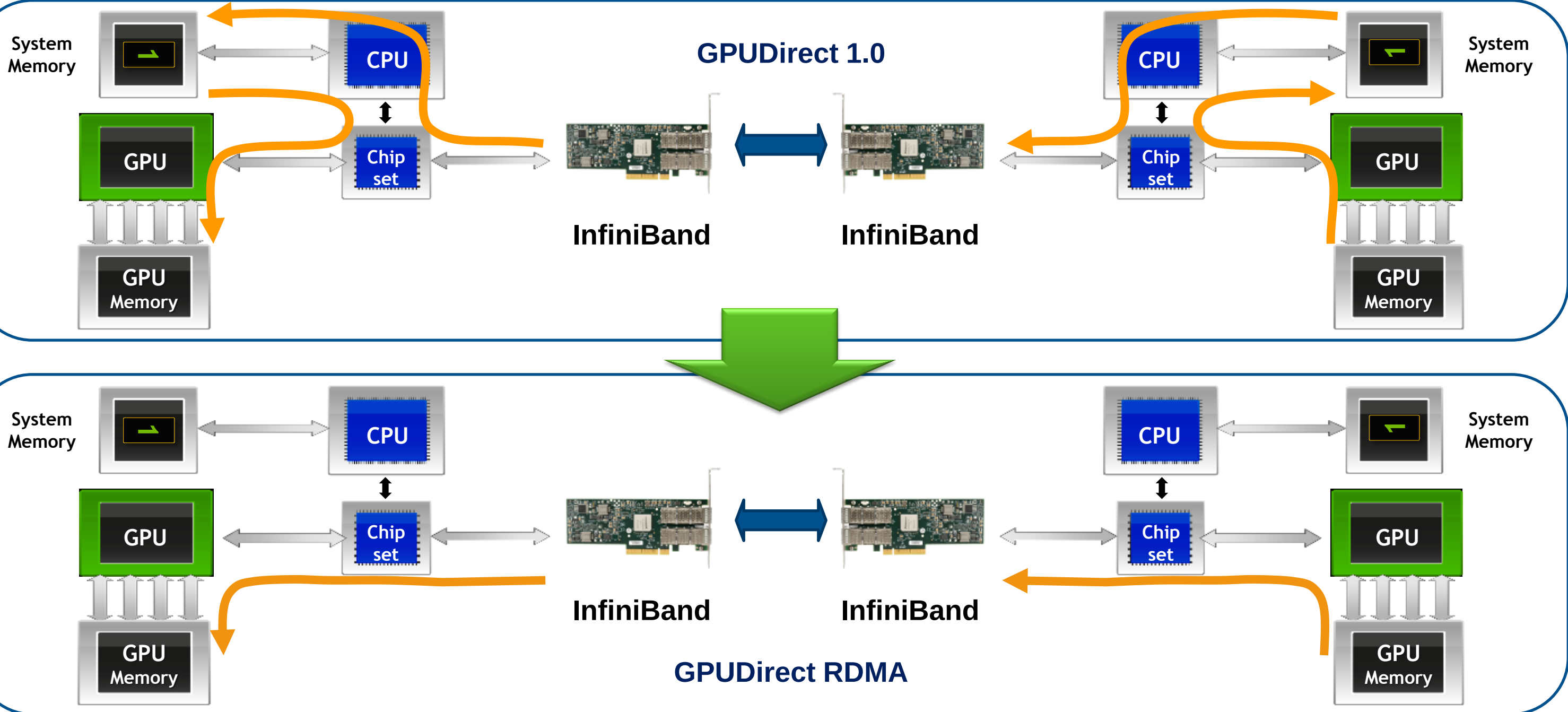
InfiniBand



GPUDirect RDMA

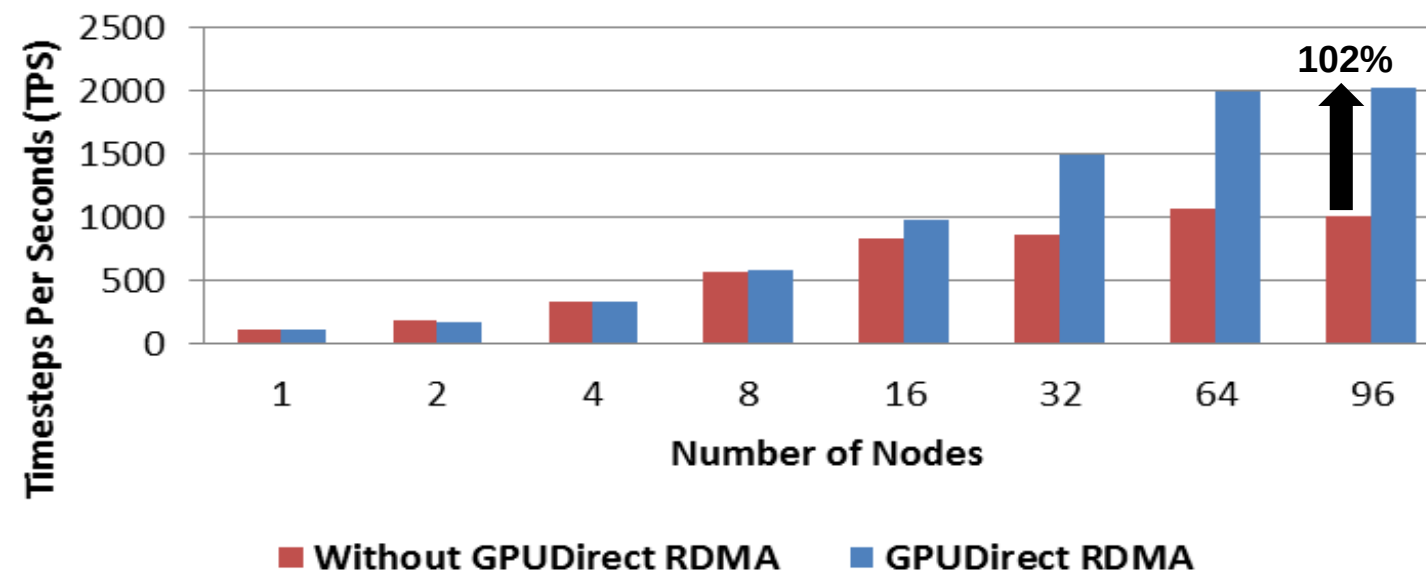
InfiniBand

InfiniBand



- HOOMD-blue is a general-purpose Molecular Dynamics simulation code accelerated on GPUs
- GPUDirect RDMA allows direct peer to peer GPU communications over InfiniBand
 - Unlocks performance between GPU and InfiniBand
 - This provides a significant decrease in GPU-GPU communication latency
 - Provides complete CPU offload from all GPU communications across the network
- Demonstrated up to 102% performance improvement with large number of particles

HOOMD-blue Performance (LJ Liquid Benchmark, 512K Particles)



HOOMD
=blue

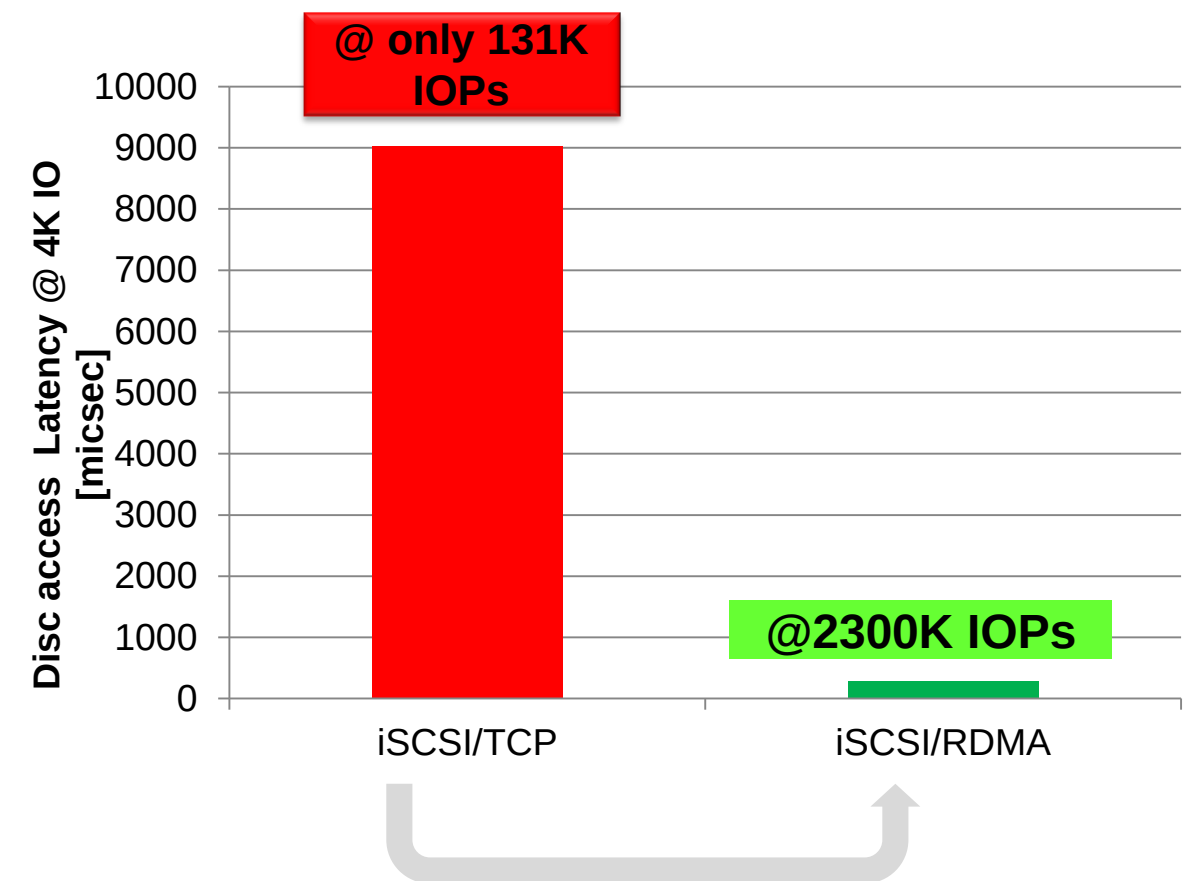
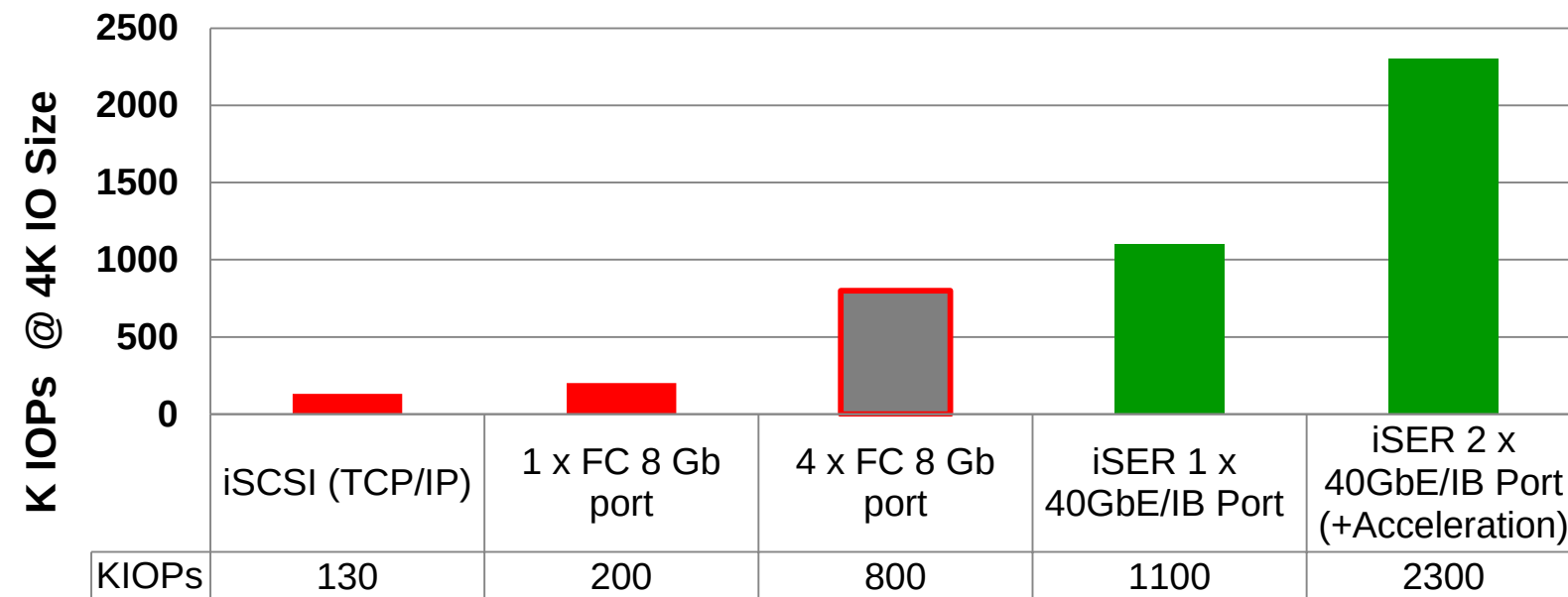


Storage

InfiniBand RDMA Storage – Get the Best Performance!



- Transport protocol implemented in hardware
- Zero copy using RDMA

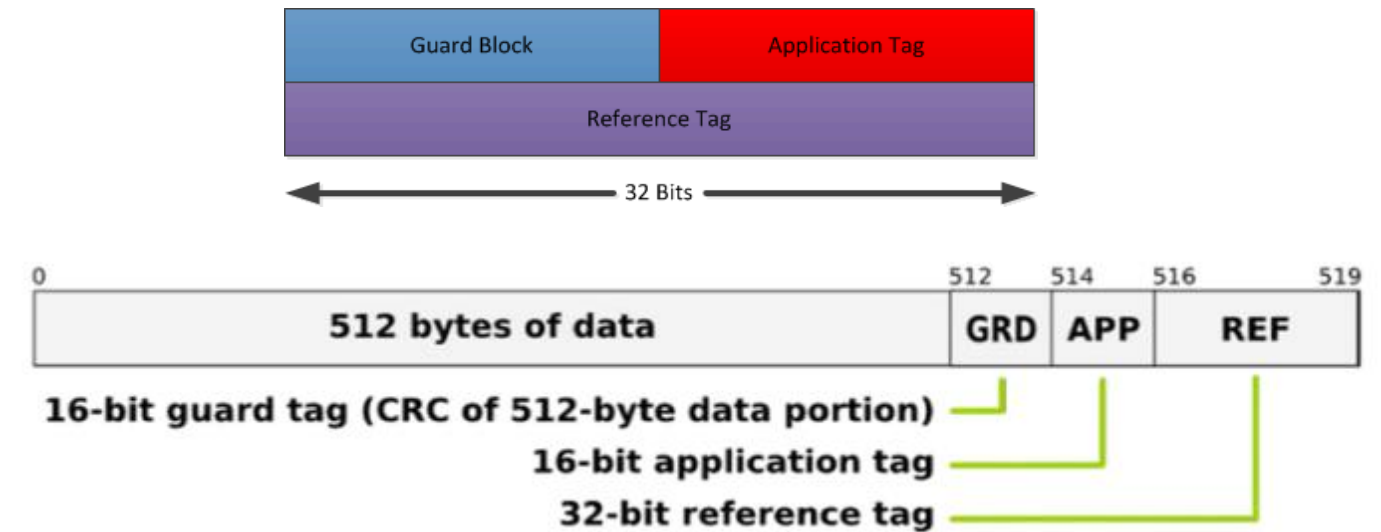
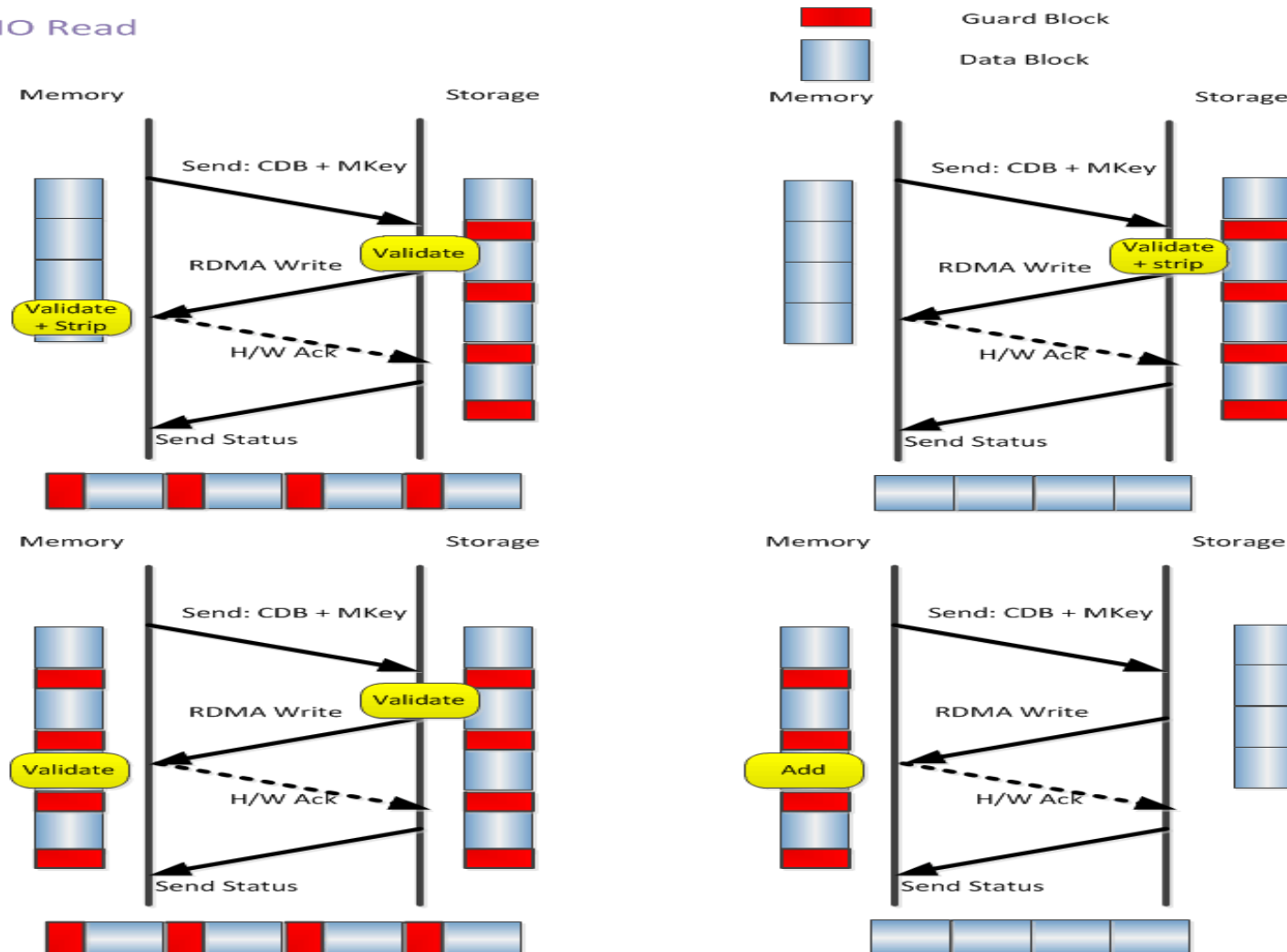


5-10% the latency under 20x the workload

Data Protection Offloaded

- Used to provide data block integrity check capabilities (CRC) for block storage (SCSI)
- Proposed by the T10 committee
- DIF extends the support to main memory

IO Read



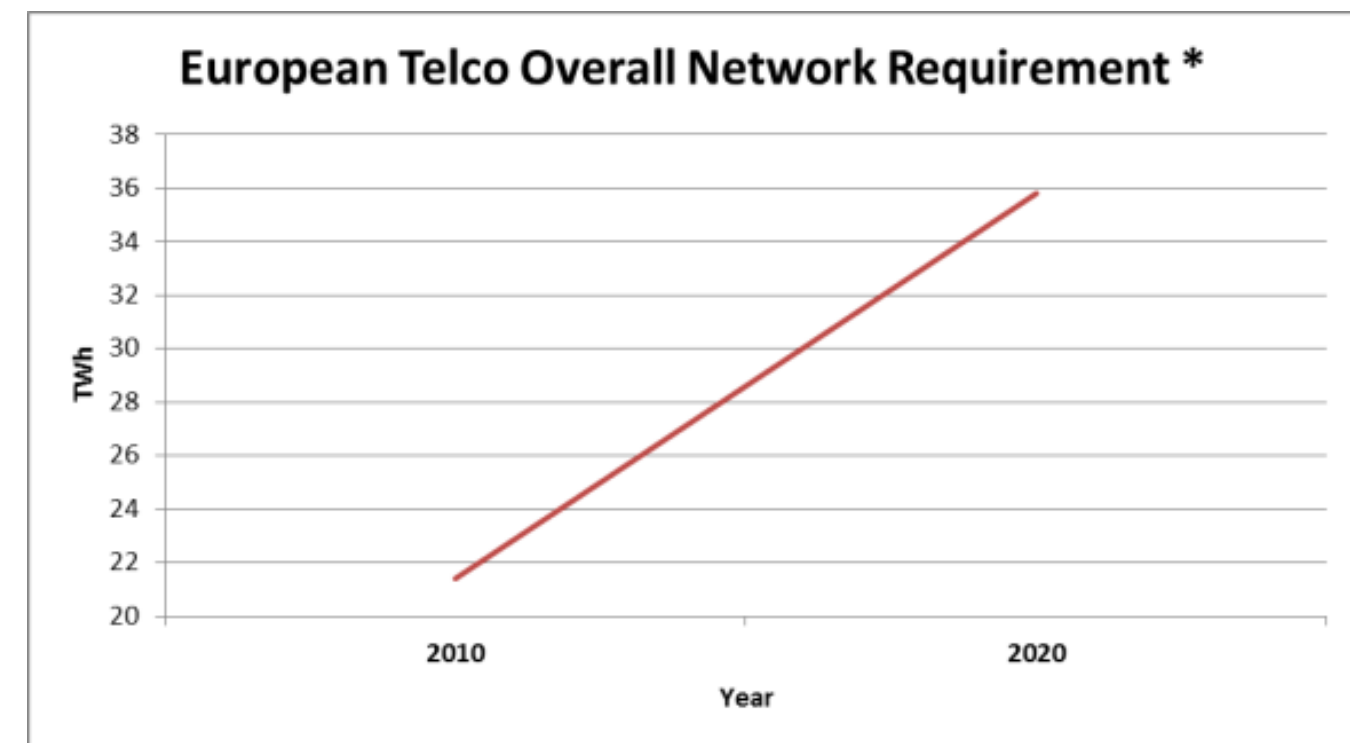


Power

Motivation For Power Aware Design

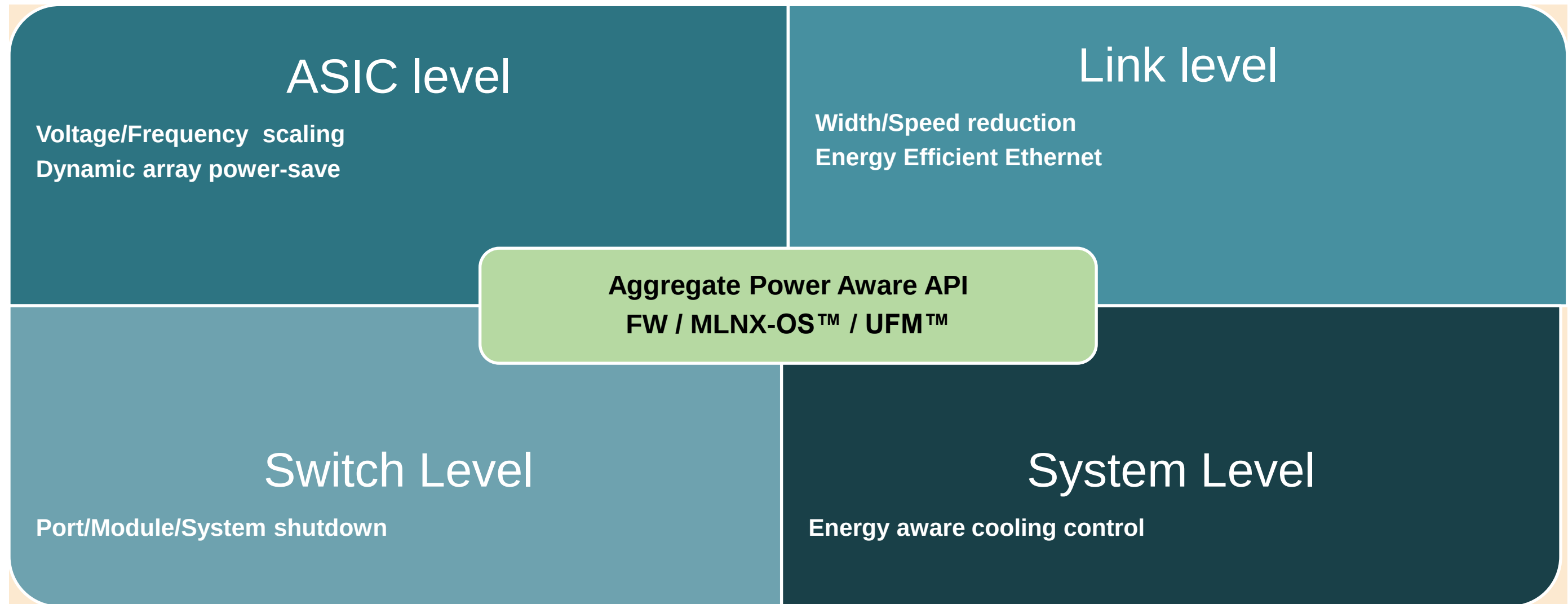
- Today networks work at maximum capacity with almost constant dissipation
- Low power silicon devices may not suffice to meet future requirements for low-energy networks
- The electricity consumption of datacenters is a significant contributor to the total cost of operation
 - Cooling costs scale as 1.3X the total energy consumption

- Lower power consumption lowers OPEX
 - Annual OPEX for 1KW is ~\$1000



* According to Global e-Sustainability Initiative (GeSI)
if green network technologies (GNTs) are not adopted

Increasing Energy Efficiency with Mellanox Switches

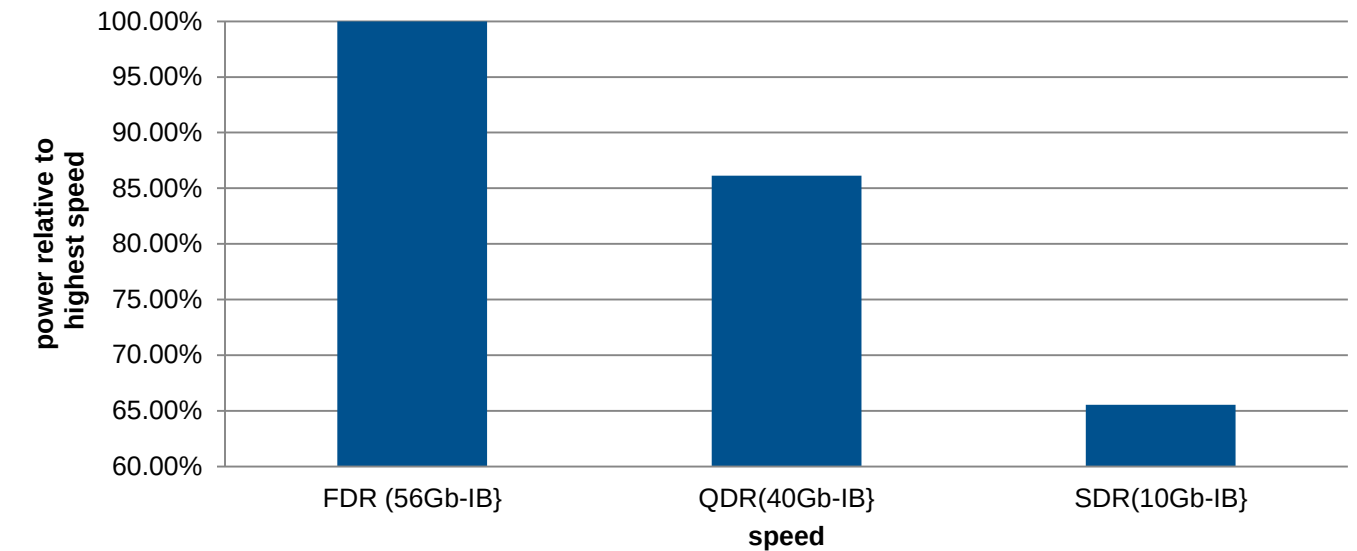


LECO net
Low Energy Consumption NETWORKs

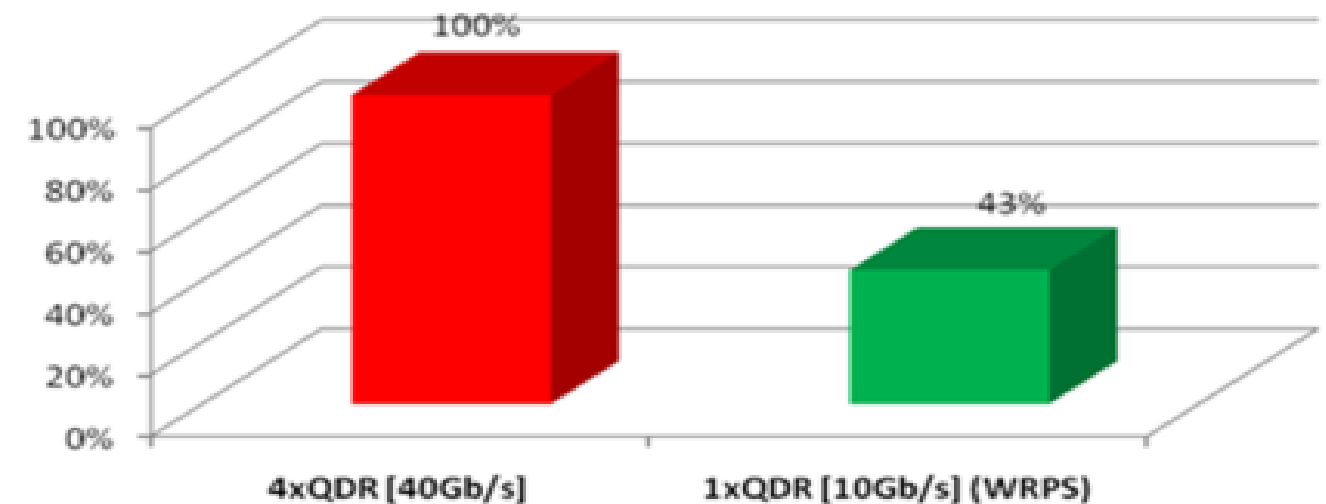
Prototype Results - Power Scaling @ Link Level



- Speed Reduction Power Save [SRPS]



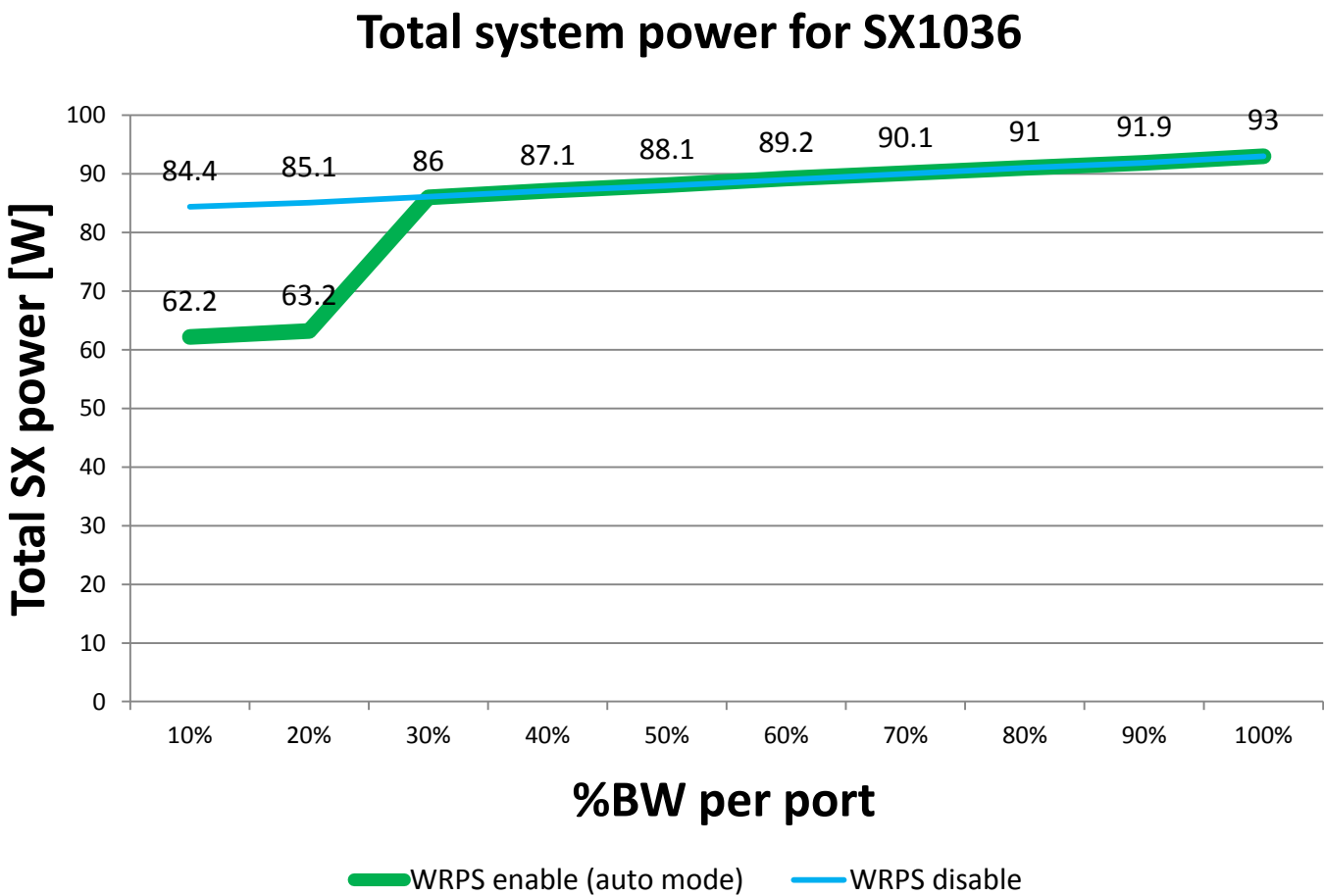
- Width Reduction Power Save [WRPS]



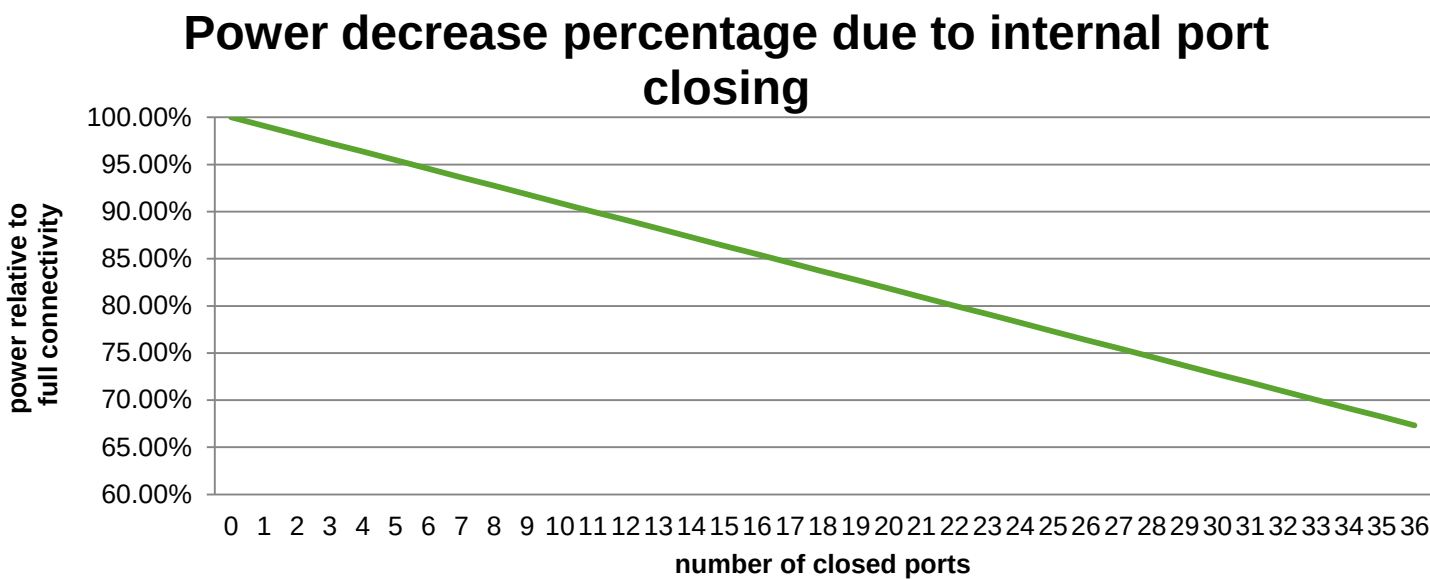
Prototype Results - Power Scaling @ System Level



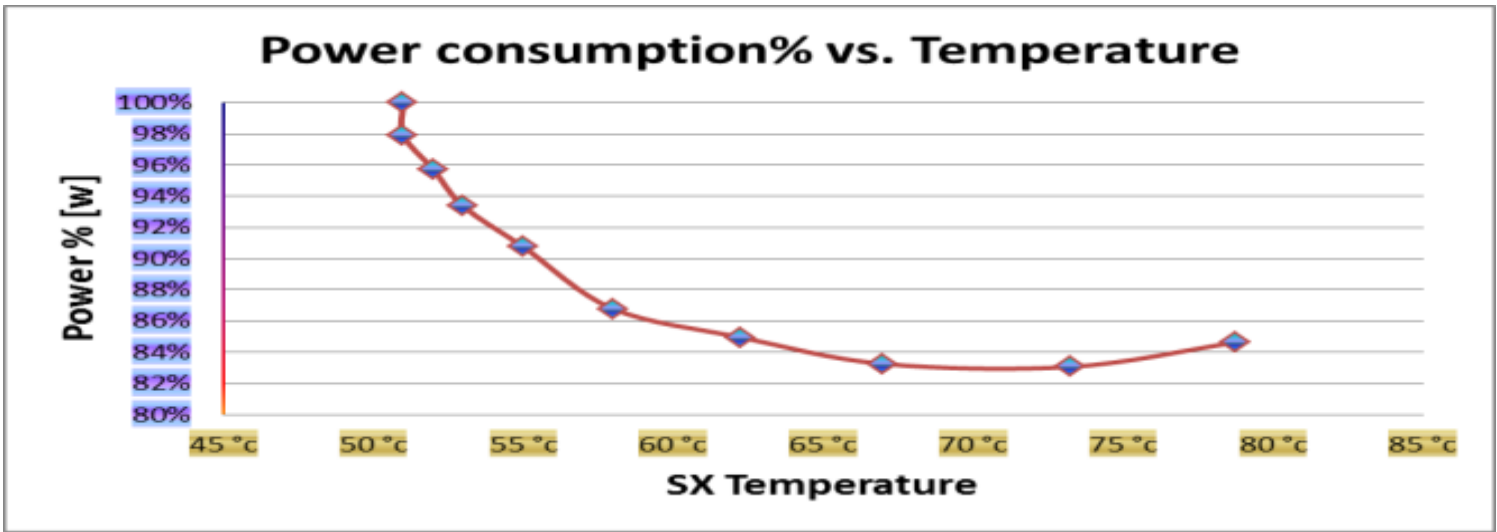
- Load based power scaling



- Internal port shutdown (Director switch) - ~1%/port



- Fan system analysis for improved power algorithm



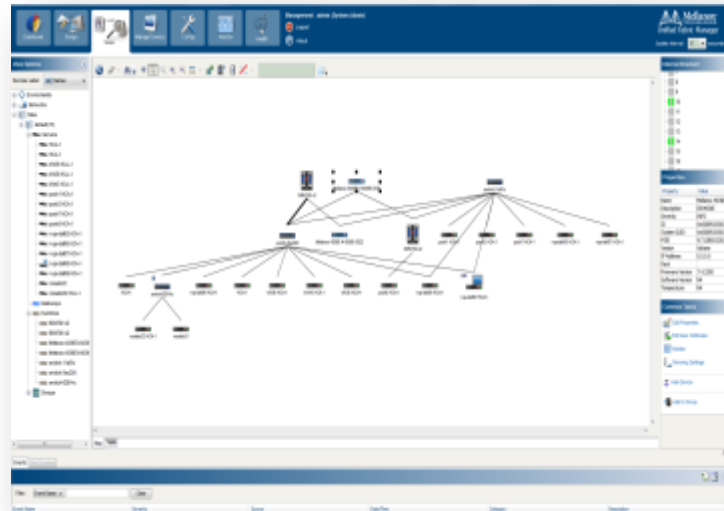


Monitoring and Diagnostics

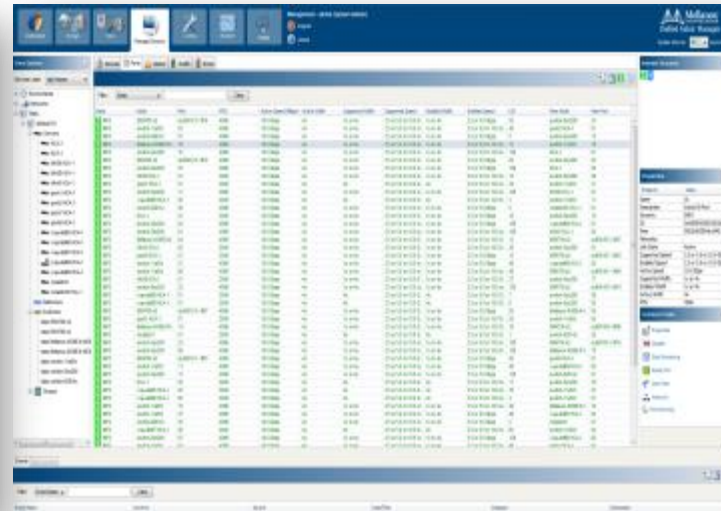
Unified Fabric Manager



Automatic Discovery



Central Device Mgmt



Fabric Dashboard



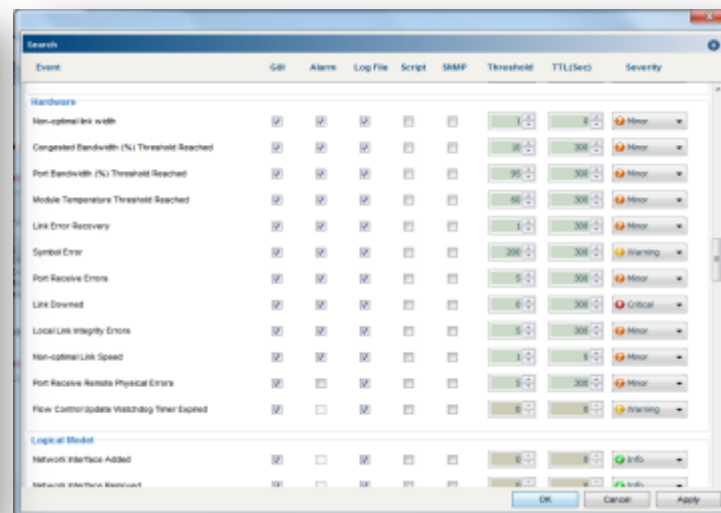
Congestion Analysis



Health & Perf Monitoring



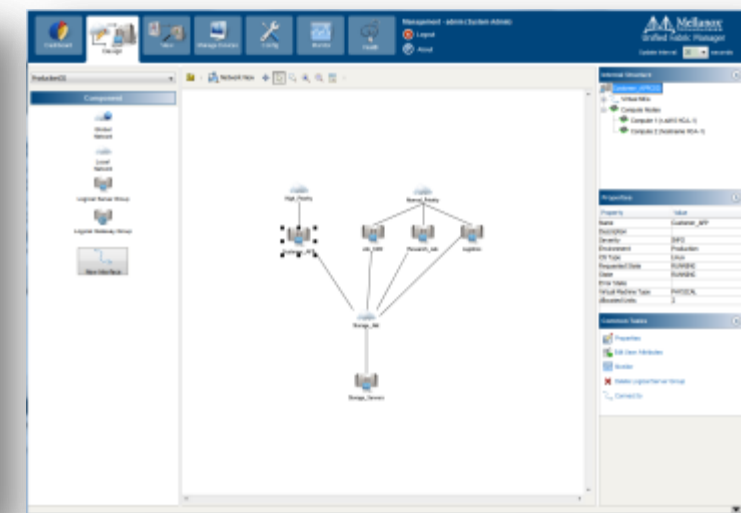
Advanced Alerting



Fabric Health Reports



Service Oriented Provisioning



ExaScale !

Mellanox InfiniBand Connected Petascale Systems

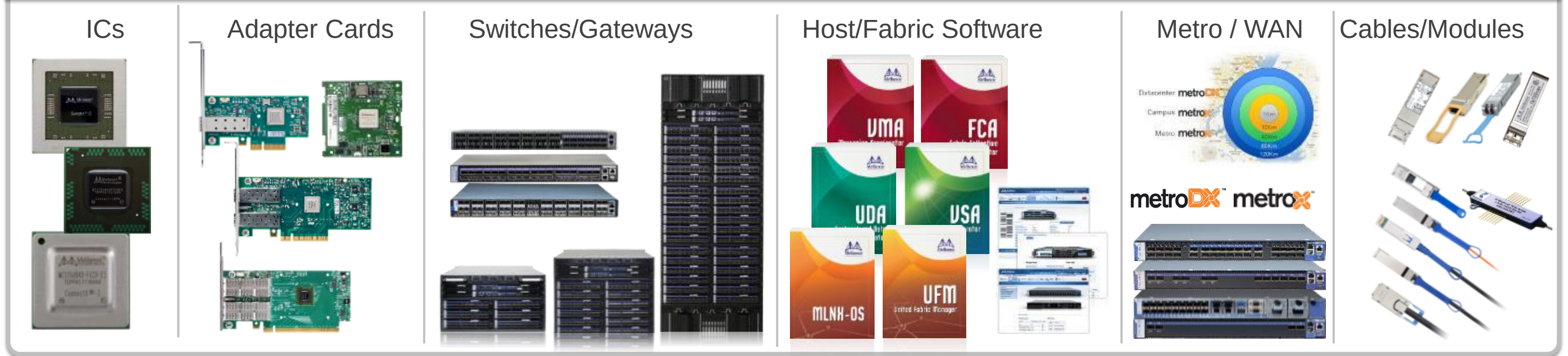


Connecting Half of the World's Petascale Systems
Mellanox Connected Petascale System Examples

The Only Provider of End-to-End 40/56Gb/s Solutions



Comprehensive End-to-End InfiniBand and Ethernet Portfolio



From Data Center to Metro and WAN

X86, ARM and Power based Compute and Storage Platforms

The Interconnect Provider For 10Gb/s and Beyond



Thank You